



When assert MRESST, RESET2 signal will be asserted as well and resend a reset signal to TW.

Notice

Connect to PCN OFF.All(CFL Platform)
Manual Reset to TR for better signal support
should be connected to EC/SOC GPIO

- 0' - No Manual Reset is being assert
- 1' - Manual Reset is being assert

I2C1 address	R1219 DIV = 0	R1219+R1230 DIV = 0.338	R1219+R1247 DIV = 0.5	R1219+R1209 DIV = 0.90
I2C1_C1_ADDR	000b	001b	010b	011b
I2C1_C2_ADDR	100b	101b	110b	111b

Table 2. IEC Default Values/Address IEC1 - Part 1

TABLE 2. PC Unique Address (UE1 - PGT 1)							
(Default PC Unique Address)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	UEC_ADDR[0:15] (UE1-UE5)		0	1

Note 1: Any bit is available for each user independently according to license scope of the PC address.

Table 3. IFC Default Unique Address DC1 - Port 2

Default PC Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	PC_ADDR_OF_CODE_C2D-H			Not

Note 1: Any bit is invariable for each port independently (providing firmware supports the PC's address).

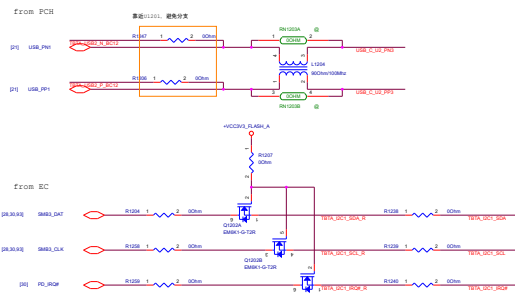
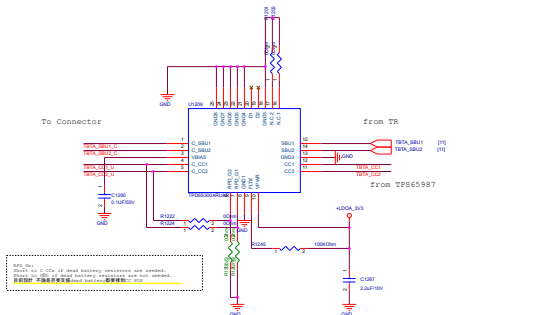
For the OGC interface, the unique PC address is a fixed value as shown in [Table 4](#) and [Table 5](#).

Table 4. I²C Default Unique Address I2C2 - Port 1

Default FC Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	0	0	0	1010

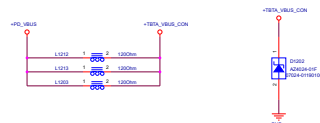
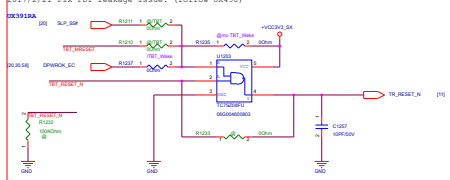
Note 1: Bit 0 is substitutable for each port independently, providing a means override of the FC address.

Power Flow Chart

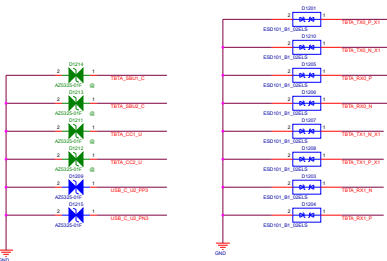
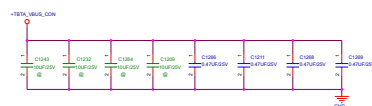
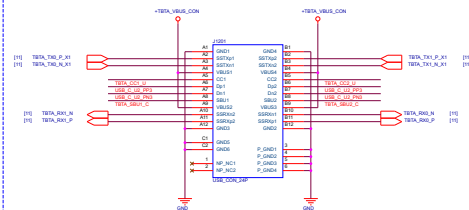


確認是否需要

2017/2/21 Fix PDI leakage issue. (follow UX490)

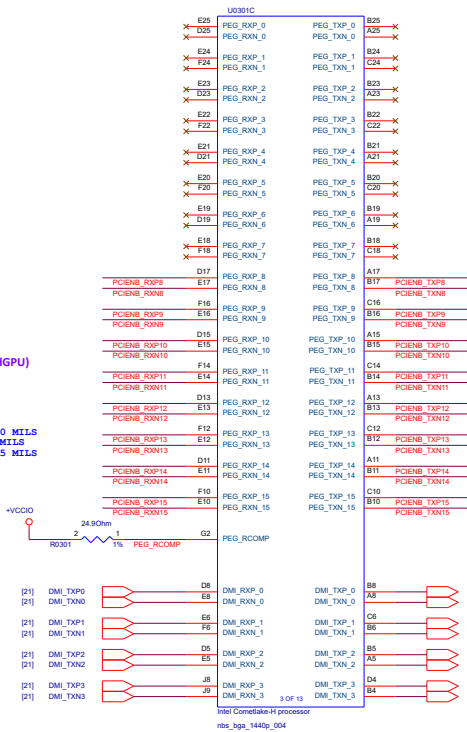


TYPE-C Connector

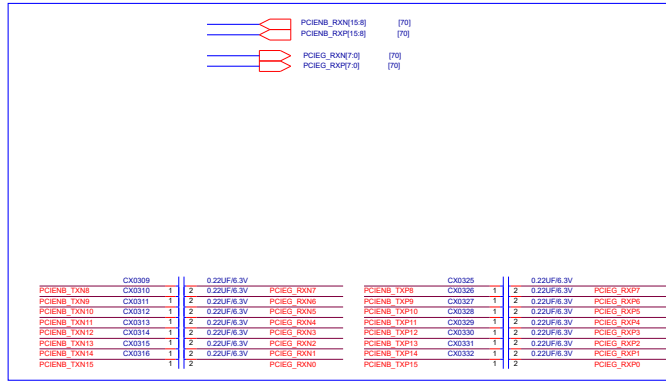


dGPU
(AC-CAP Place on dGPU)

Trace length < 400 MILLS
Trace width = 12 MILLS
Trace spacing = 15 MILLS



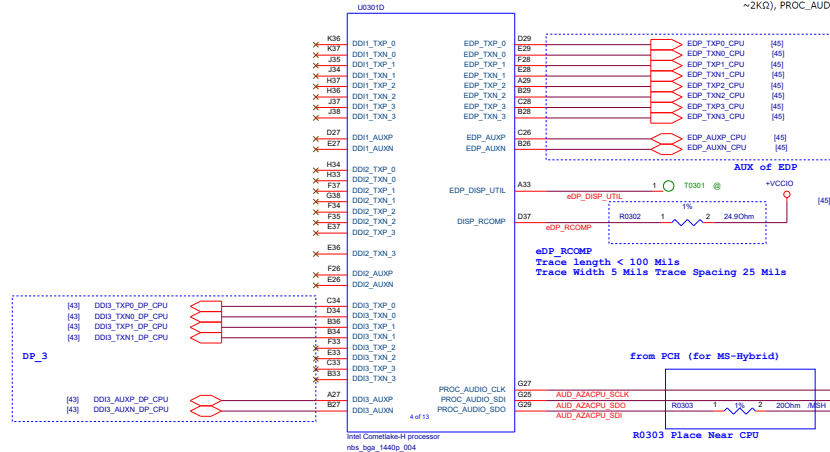
R0.1-25



CPU i7 / i9, 共用線路, 用BOM區分
CPU料號如下
I7-10750H : 01001-01860400
I9-10880H : 01001-01860500

Display

2017/11/16 Add HDMI/TBT/eDP interface for MS-Hybrid by James

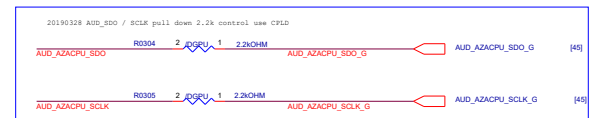
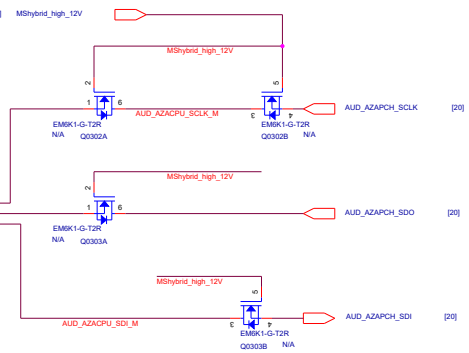


Add for 2nd Display 0419

31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ). PROC_AUDIO_SDO can be left unconnected.



Refer to CML-H PDG P.339 (Doc.611586)

Disabling and Termination Guidelines for the Intel High Definition Audio Interface and the Intel Display Audio Interface

When the Intel HD Audio interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI on the CPU need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ), PROC_AUDIO_SDO on the CPU can be left unconnected. The Intel Display Audio pins on the PCH may be left disconnected.

Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes													
				0	1	2	3	4	5	6	7	8	9	10	11	12	13
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2

- Notes:**
- Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
 - In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
 - Connect lane 0 of 1st device to lane 0.
 - Connect lane 0 of 2nd device to lane 8.
 - Connect lane 0 of 3rd device to lane 12.
- For example:
- When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
 - When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
 - When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane12.

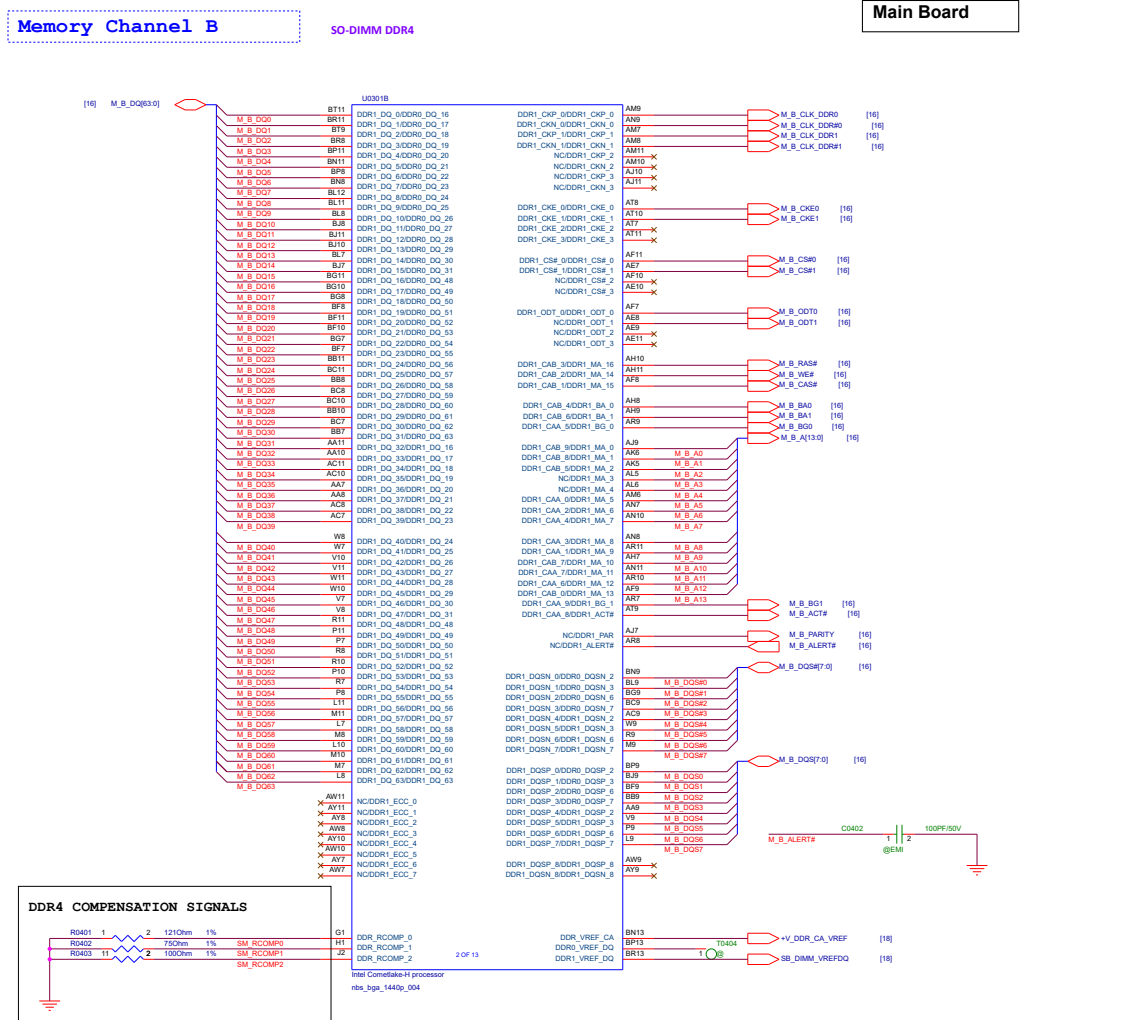
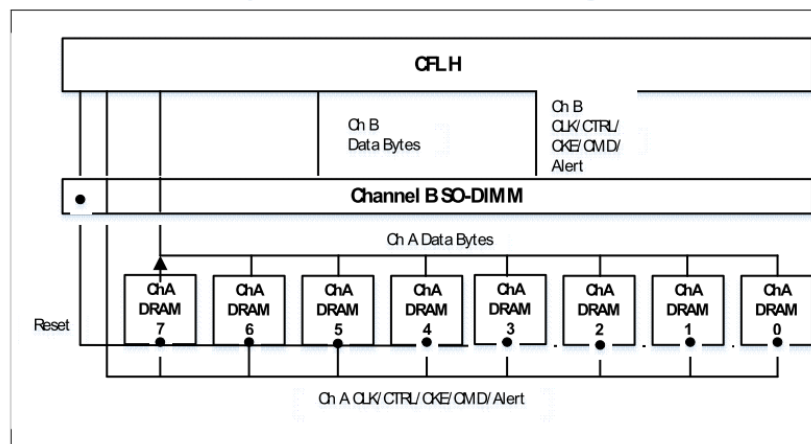
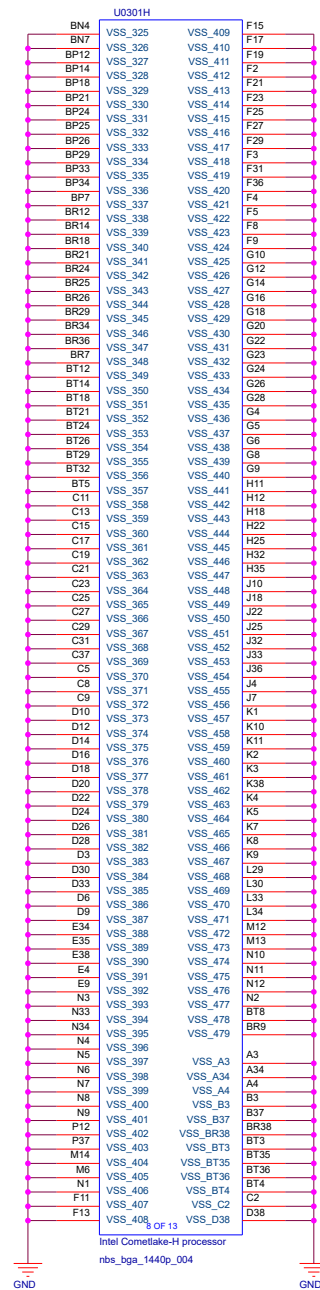
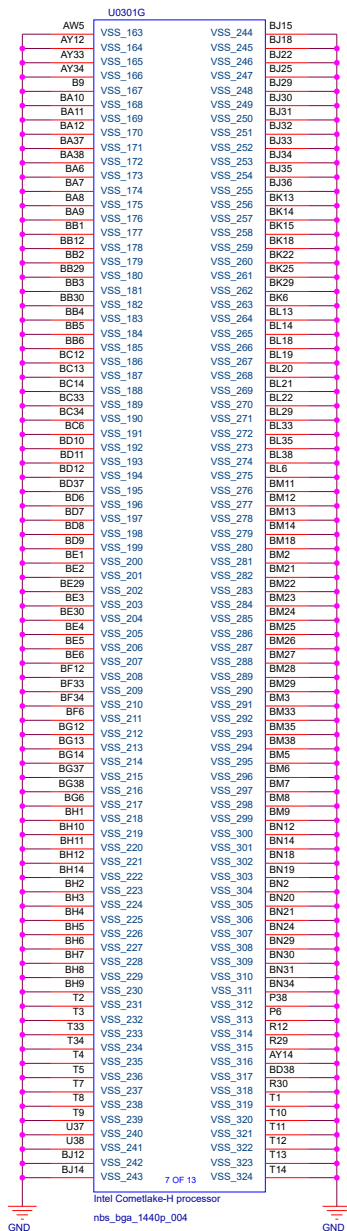
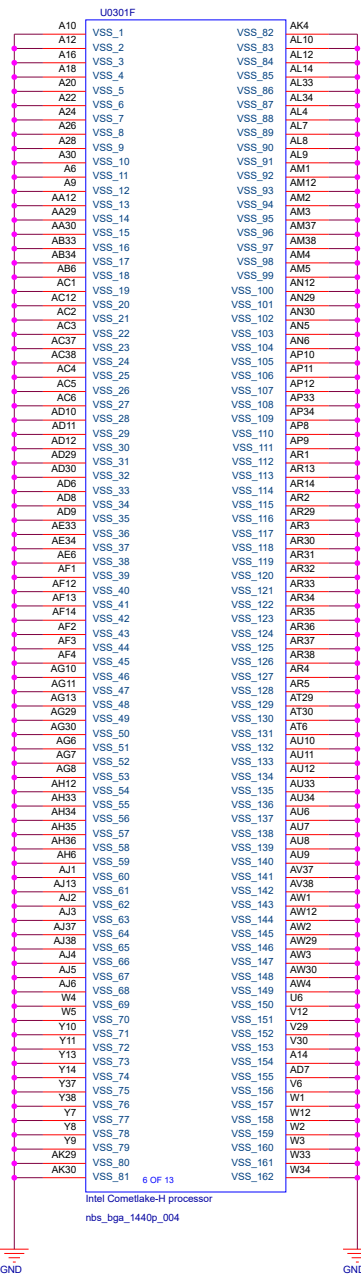




Figure 4-16. CFL-H DDR4 x8 Memory Down Placement and Block Diagram





		Title : DDR4_TERMINATION	
ASUSTeK COMPUTER INC.		Engineer: EE	
Size A	Project Name GX550LXS		Rev R1.2
Date: Wednesday, February 19, 2020		Sheet 13 of 99	

		Title : DDR4_ON-BOARD_A2	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX550LXS		Rev R1.0
Date: Wednesday, February 19, 2020		Sheet 15 of 103	


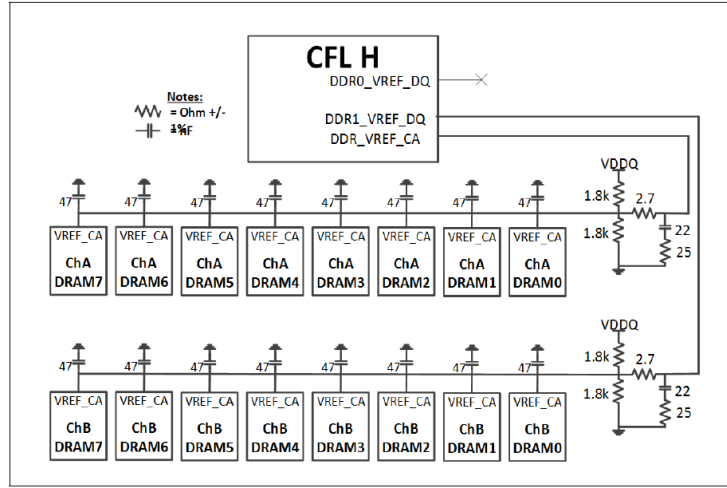
		Title : NB_****	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX550LXS		Rev R1.0
Date: Wednesday, February 19, 2020		Sheet 17 of 103	

Figure 4-24. CFL-H DDR4 x8 Memory Down V_{REF-CA} Overview



Memory Down Vref

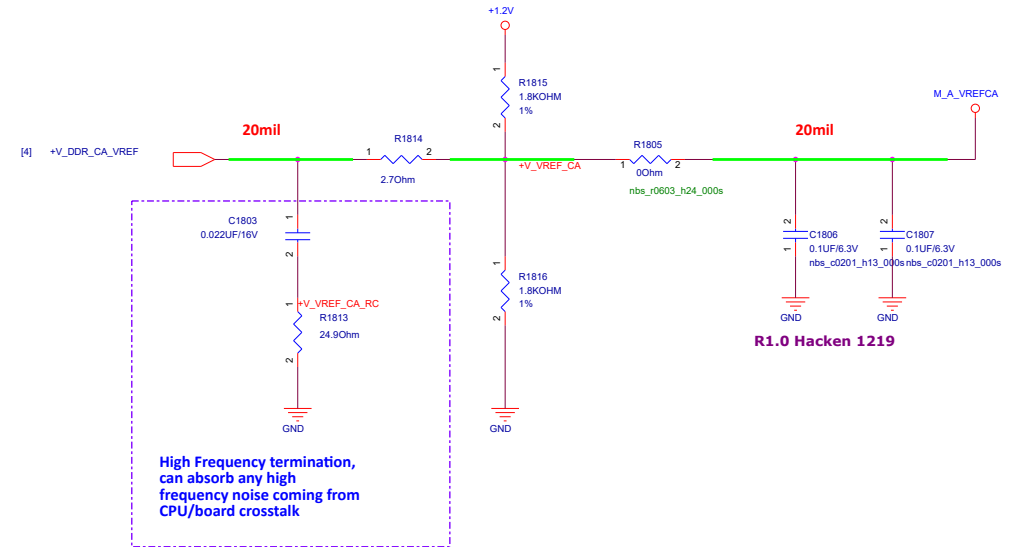
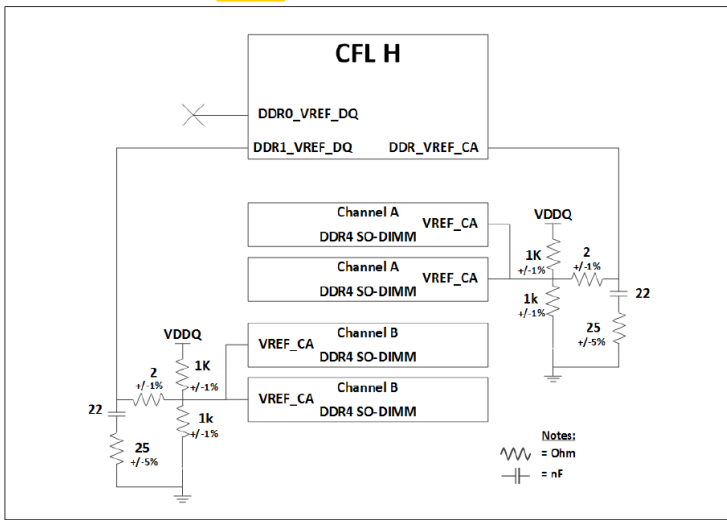
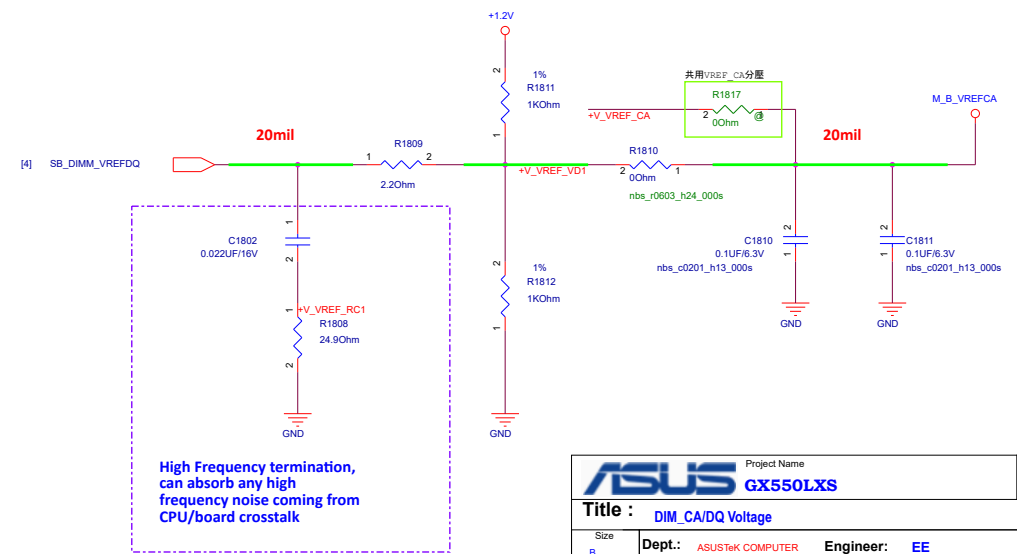
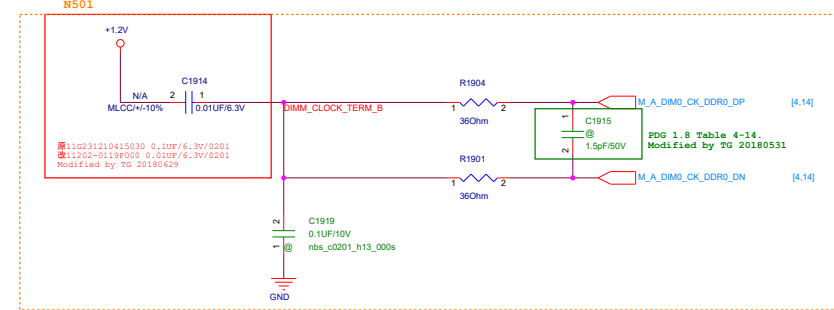
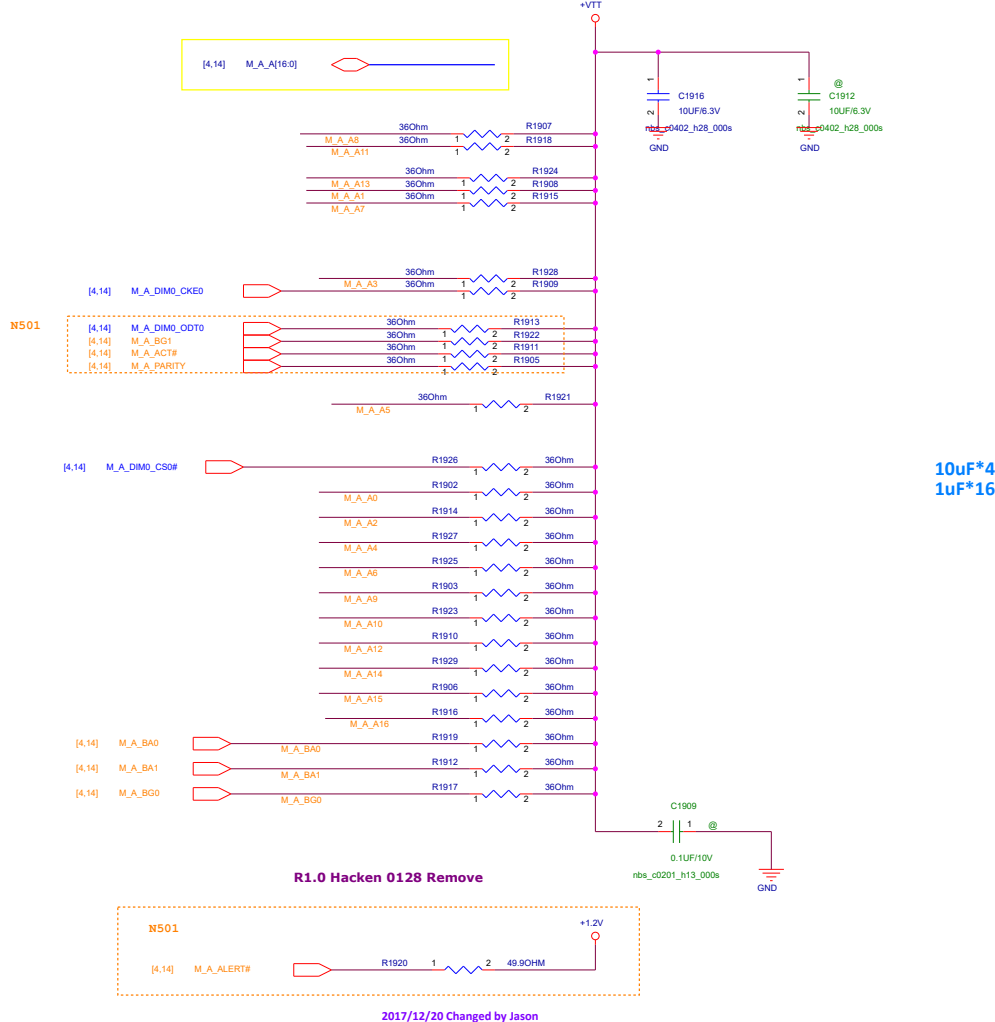


Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview



SO-DIMM1 Vref





Clock Pull up power change from +0.6V to +1.2V (CFL PDG) 20820601

10uF*4
1uF*16

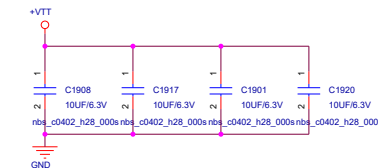
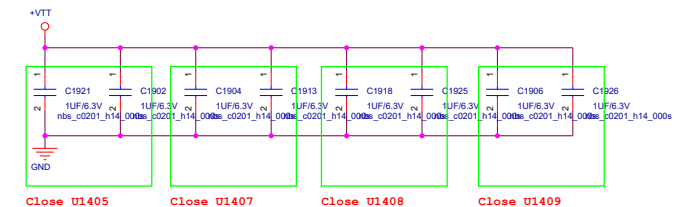
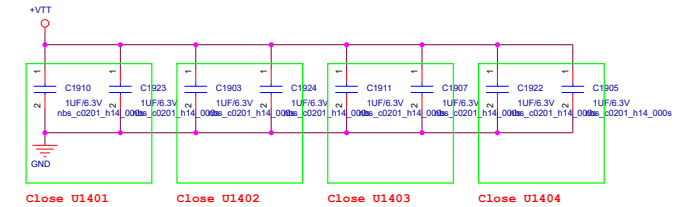


Table 4-25. DDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)	Note
DDR4 Memory Down x8- 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x8 DRAM device as possible	64x 1 μ F (0402) (min of 48 stuffed)	
		Distributed around the DRAM devices	20x 10 μ F (0603) (min of 12 stuffed)	
	VPP	2 as near each x8 DRAM device as possible	32x 1 μ F (0402)	
		Distributed around the DRAM devices	10x 10 μ F (0603)	
	VTT	Distributed along termination resistors	32x 1 μ F (0402)	
		Distributed evenly across domain	8x 10 μ F (0603)	

<Core Design>

Setting

GX502GX PCIe/SATA Function define

CNL HM370 (PCIe#1-PCIe#8 not support)

HSIO Capabilities

Function

Function

CLKREQ-0

GPU

CLKREQ-1

CLKREQ-2

WLAN

CLKREQ-3

CLKREQ-4

GLAN

CLKREQ-5

CLKREQ-6

SSD1

CLKREQ-7

CLKREQ-8

SSD2

CLKREQ-9

CLKREQ-10~15

PCIeR11- SATA-0a

PCIeR12- SATA-1a

PCIeR13- SATA-0b

PCIeR14- SATA-1b

PCIeR15 / SATA#2

GLAN

PCIeR16 / SATA#3

WLAN

PCIeR17 / SATA#4

PCIeR18 / SATA#5

PCIeR19 / SATA#6

PCIeR20 / SATA#6

PCIeR21

PCIe21_SSD_P0

PCIeR22

PCIe22_SSD_P1

PCIeR23

PCIe23_SSD_P2

PCIeR24

PCIe24_SSD_P3

USB Setting

GX502GX USB Function define

CNL HM370 (only #1-#4 support GEN2)

USB 2.0

Function

Function

USB2_01

(Port1)USB3.1 Gen2 TypeC

USB2_02

USB2_03

(Port3)USB3.1 Gen2 TypeA

USB2_04

(Port1)USB3.1 Gen2 TypeA

USB2_05

(Port2)USB3.1 Gen2 TypeA

USB2_06

USB2_07

USB2_08

USB2_09

USB2_10

N key

USB2_11

USB2_12

USB2_13

USB2_14

BT

USB 3.0

Function

Function

USB3.1I01

(Port1)USB3.1 Gen2 TypeA

USB3.1I02

(Port2)USB3.1 Gen2 TypeA

USB3.1I03

(Port1)USB3.1 Gen2 TypeA

USB3.1I04

(Port1)USB3.1 Gen2 TypeC

USB3.1I05

USB3.1I06

USB3.1I07

USB3.1I08

HSIO

HM370

QM370

CM246

IRST

Devices Assign

GX502GX組態(0928)

0

USB3.1 Gen2/S0 #1

USB3.1 Gen2/S0 #1

USB3.1 Gen2/S0 #1

Gen2/1 USB3.1 Type C

(Port1)USB3.1 Gen2 TypeA

1

USB3.1 Gen2/S0 #2

USB3.1 Gen2/S0 #2

USB3.1 Gen2/S0 #2

Gen2/1 USB3.1 Type C

(Port2)USB3.1 Gen2 TypeA

2

USB3.1 Gen2/S0 #3

USB3.1 Gen2/S0 #3

USB3.1 Gen2/S0 #3

Gen2/1 USB3.1 Type A

USB3.1 Type A

3

USB3.1 Gen2/S0 #4

USB3.1 Gen2/S0 #4

USB3.1 Gen2/S0 #4

Gen2/1 USB3.1 Type A

USB3.1 Type A

4

USB3.1 Gen2/S0 #5

USB3.1 Gen2/S0 #5

USB3.1 Gen2/S0 #5

Gen2/1 USB3.1 Type A

USB3.1 Type A

5

USB3.1 Gen2/S0 #6

USB3.1 Gen2/S0 #6

USB3.1 Gen2/S0 #6

Gen2/1 USB3.1 Type A

USB3.1 Type A

6

USB3.1 Gen2/S0 #7

USB3.1 Gen2/S0 #7

PCIe #5

CR (USB3.0 / PCIe)

7

USB3.1 Gen2/S0 #8

USB3.1 Gen2/S0 #8

PCIe #2

8

NA

USB3.1 Gen2/S0 #9

PCIe #3

9

NA

USB3.1 Gen2/S0 #10

PCIe #4

10

NA

PCIe #5

PCIe #5

11

NA

PCIe #7

PCIe #5

12

NA

PCIe #7

PCIe #5

13

NA

PCIe #8

PCIe #5

14

PCIe #9

PCIe #9

PCIe #9

15

PCIe #10

PCIe #10

PCIe #10

16

PCIe #11

SATA #0

PCIe #11

Yes

17

PCIe #12

SATA #1

PCIe #12

Yes

18

PCIe #13

SATA #2

PCIe #13

Yes

19

PCIe #14

SATA #3

PCIe #14

Yes

20

PCIe #15

SATA #4

PCIe #15

Yes

21

PCIe #16

SATA #5

PCIe #16

Yes

22

PCIe #17

SATA #6

PCIe #17

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SATA #6

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PCIe #19

SATA #6

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Yes

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PCIe #20

SATA #7

PCIe #20

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PCIe #21

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PCIe #184

PCIe #184

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PCIe #185

PCIe #185

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PCIe #186

PCIe #186

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PCIe #187

PCIe #187

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PCIe #188

PCIe #188

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PCIe #189

PCIe #189

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PCIe #190

PCIe #190

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PCIe #191

PCIe #191

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PCIe #192

PCIe #192

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PCIe #193

PCIe #193

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PCIe #194

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PCIe #195

PCIe #195

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PCIe #196

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PCIe #201

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PCIe #202

PCIe #202

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PCIe #203

PCIe #203

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PCIe #204

PCIe #204

210

PCIe #205

PCIe #205

211

PCIe #206

PCIe #206

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PCIe #207

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PCIe #208

PCIe #208

214

PCIe #209

PCIe #209

215

PCIe #210

PCIe #210

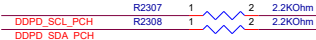
216

PCIe #211

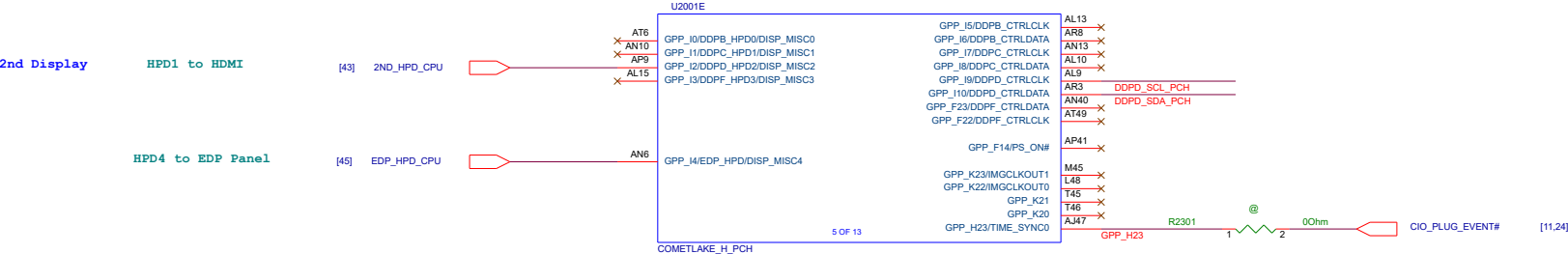
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Main Board

- HPD0 to DP
- HPD1 to HDMI
- HPD2 to TBT
- HPD3 to VGA
- HPD4 to EDP Panel



DDP Strap Setting Update:
0 = Port is not detected (Default)
1 = Port is detected



DDP Strap Setting Update:
0 = Port is not detected (Default)
1 = Port is detected

GPP_I6 / DDPB_CTRLDATA	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. Notes: 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I8 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. Notes: 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I10 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. Notes: 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_F23	Display Port F Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected. Notes: 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well. 3. This strap applies to platforms that support Display Port F only. Refer to the platform's processor documentation for info on Display Port F support.

5.6

Digital Display Interface Disabling and Termination Guidelines

All the digital display ports on the Coffee Lake processor have a strap associated with it. The port strap needs to be set to configure each digital port irrespective of the digital display technology HDMI/DP. The following table lists all the digital display straps and guidelines to enable/disable a respective port on the platform. All the straps are sampled on the rising edge of the PWROK signal.

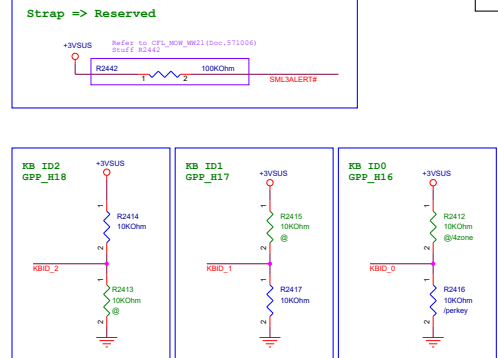
Table 5-15. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable PortΩ	How to Disable PortΩ
Port 1	DDPB_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect
Port 3	DDPD_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect

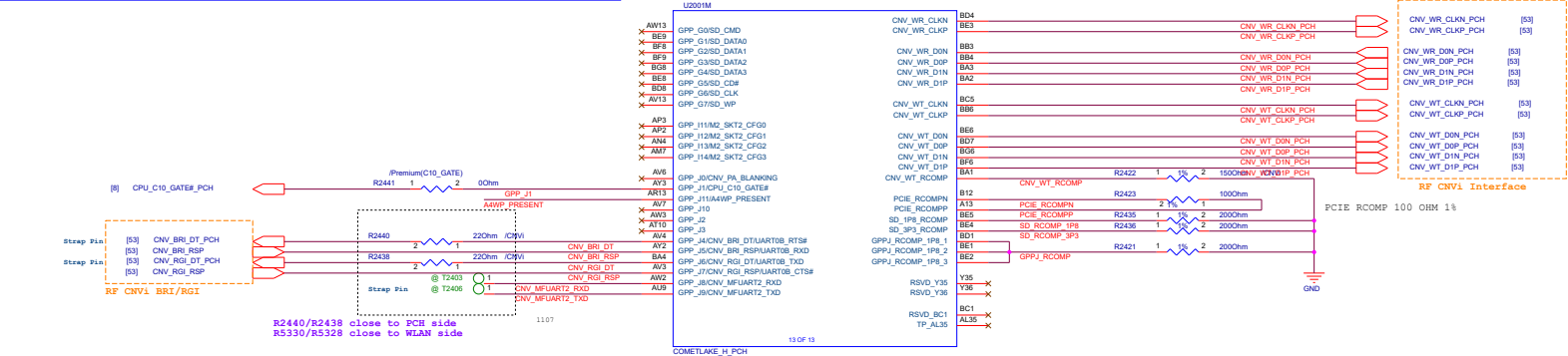
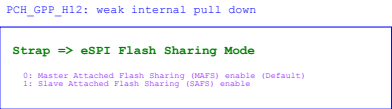
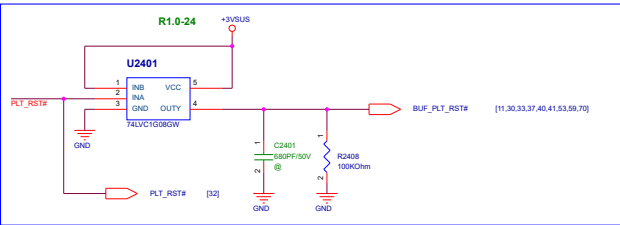
DDI Ports Availability

Ports	Port name in VBT	U-Processor Line ^{4,5}	H-Processor Line ^{4,5}	S-Processor Line ^{4,5}
DDI0 - eDP	Port A	Yes	Yes	Yes
DDI1	Port B	Yes	Yes	Yes
DDI2	Port C	Yes	Yes	Yes
DDI3	Port D	No ⁴	Yes	Yes
DDI4 - eDP/VGA	Port E	No	Yes ¹	Yes ¹

Notes:
1. For more information please see Section 2.5.2, "eDP* bifurcation."
2. 3xDDC (DDPB, DDPC, DDPD) are valid for all the processor SKUs (for U-Processor Line DDC signals description, refer to PCH EDS (See Related Document section).
3. 5xHPD (PCH) inputs (eDP_HP0, DDPB_HP00, DDPD_HP01, DDPD_HP02, DDPE_HP03) are valid for all processor SKUs.
4. No Port D for U-Processor Line. DDI3_AUX exists as reserved.
5. VBT provides a configuration option to select the four AUX channels A/B/C/D for a given port, based on how the aux channel lines are connected physically on the board.



KB ID PCH Side(HW請依照此表格做設計判斷) *BIOS會再反向				
Code	ROG RGB KB Type	KBID 2	KBID 1	KBID 0
		(GPP_H18)	(GPP_H17)	(GPP_H16)
0x00	Normal Keyboard	H	H	H
0x01	QWERTASD Partition Keyboard	H	H	L
0x02	4 Zone RGB Keyboard	H	L	H
0x03	Per Key RGB Keyboard	H	L	L
0x04	1 Zone RGB Keyboard	L	H	H



```
GPP_J4(CNV,BRI D7)
This signal has a weak internal pull down.
0 = 38.4MHz XTAL frequency selected.(Default)
1 = 24MHz XTAL frequency selected.

(MCW39)
Pin Strap for XTAL frequency selection
An external 4.7K PU to VCC(1.8V or 3.3V) is required
on this strap for PCR 24 MHz XTAL operation
```

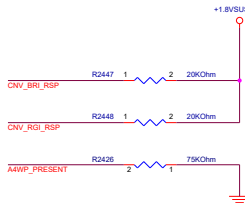
```
GPP_J6(CNV, RGI_DT):
An external pull-up or pull-down is required.
0 = Integrated CNVI enable.
1 = Integrated CNVI disable.
[Intel FAE]
RGI_DT has an automatic detect CNVI mechanism,
please do not use external PD.
The CRF has an internal strong 1K PD already.
Do not leave this pin float,
if CNVI is not used, it still need a 20K ohm PU.
```

```
GPP_J9:
The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail
```

Strap

GPP_J4(CNV_BRI_DT):Must PU 4.7K

GPP_J6(CNV_RGI_DT):Must PU 20K



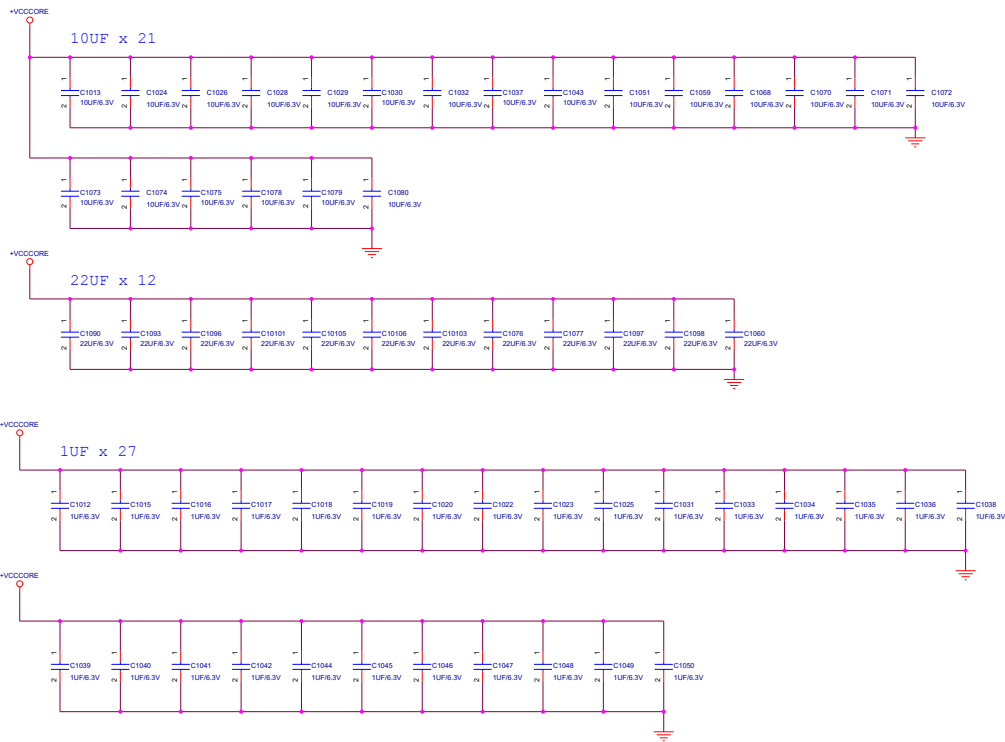
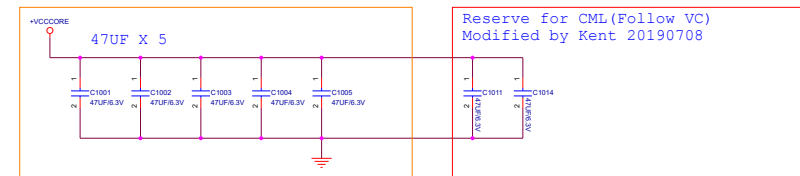
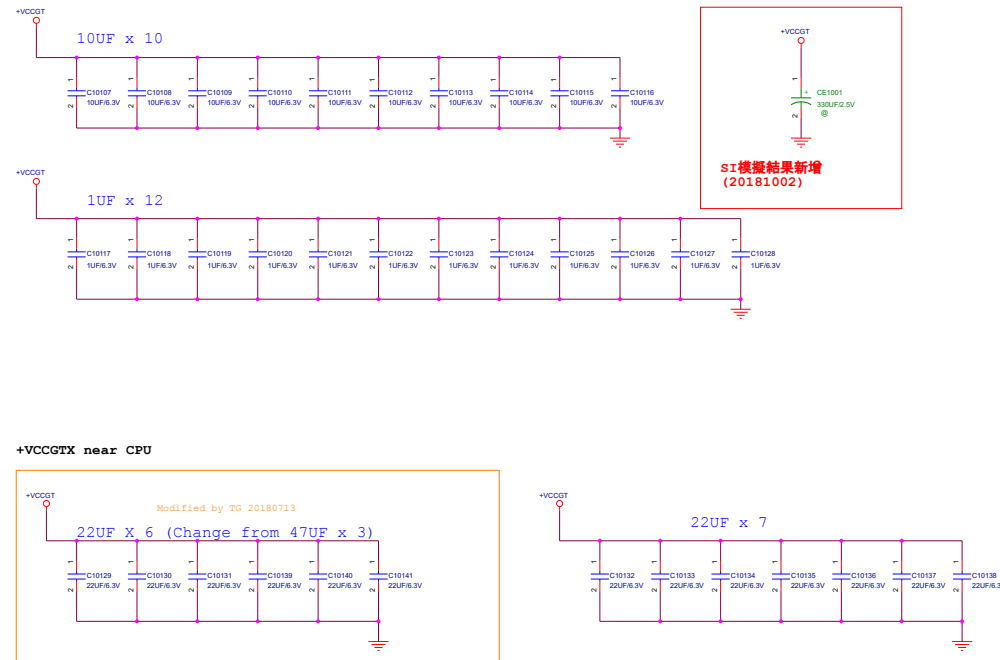
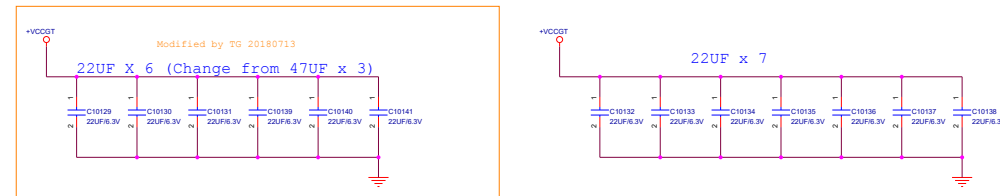
Strap => Reserved

Refer to CPL-B RVP R1.0 (Doc. 571483)

External pull-up is required. Recommended 100K if pulled up to 3.3V or 33k if pulled up to 1.8V.

```

graph TD
    SUS[3V3SUS] --- R2443[R2443  
100KOhm]
    R2443 --- R2445[R2445  
4.7KOhm]
    R2445 --- GND[Ground]
    SPI_S1[SPI_S1] --- Node(( ))
    Node --- R2443
    Node --- R2445
  
```


+VCCORE DECAPS Place Back Side (TOP)**+VCCORE near CPU****+VCCGT DECAPS Place Back Side (TOP)****+VCCGTx near CPU**

Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
Vcc _{GT}	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	

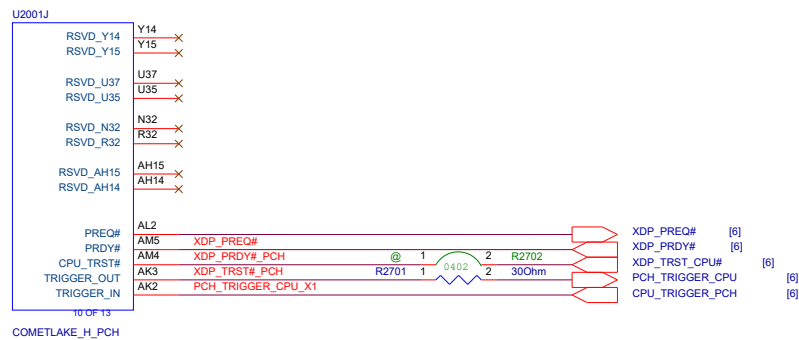
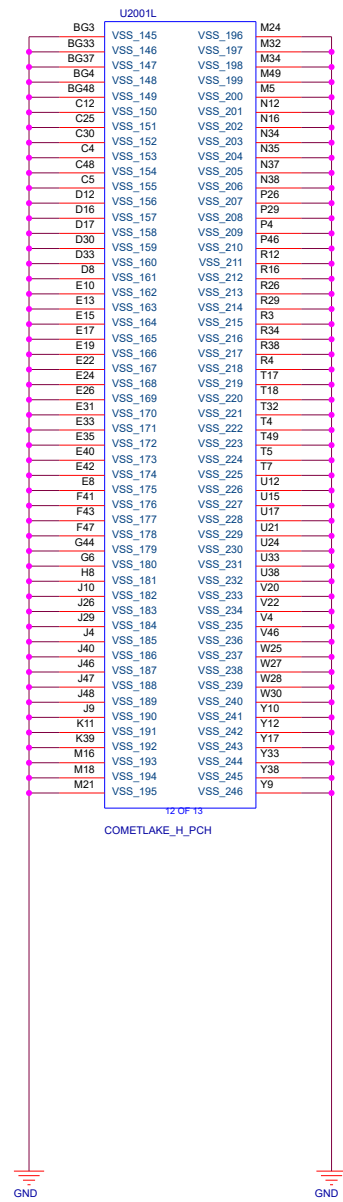
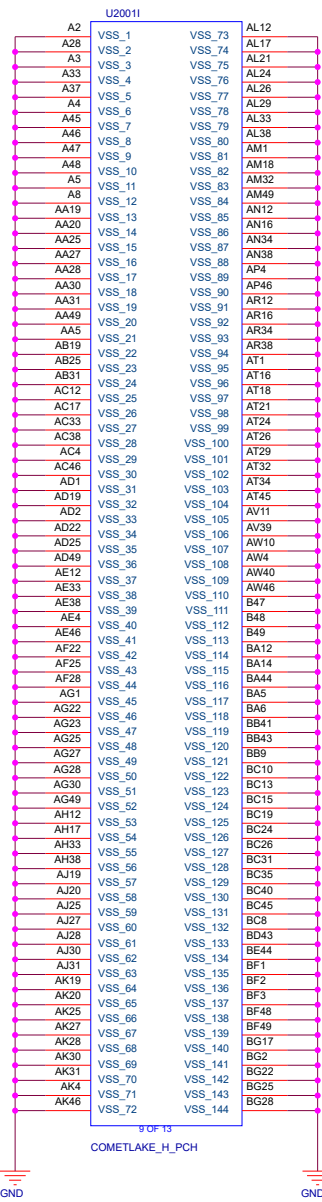


Refer to CNL-W PCR EDG R1.0 (Doc.571182)

VCCDPHY_1P24	1.24V for CNVi logic. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Cannon Lake -U/Y PDG for implementation details.
--------------	---

Purple reference CRB
Blue reference EDS





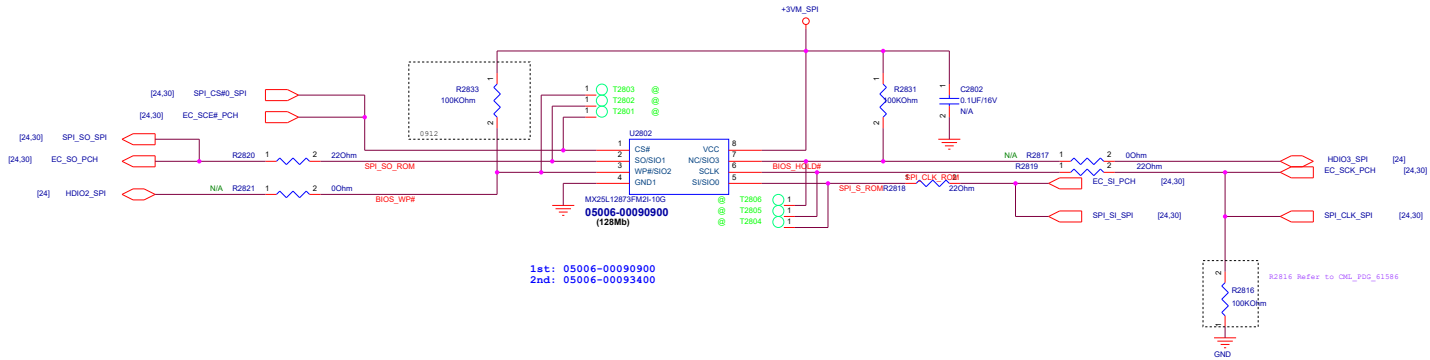
SPI Power



1st SPI ROM

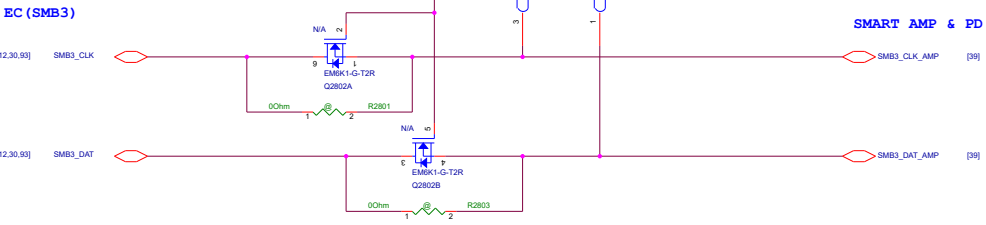
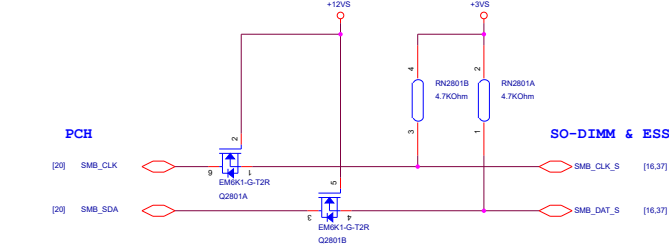
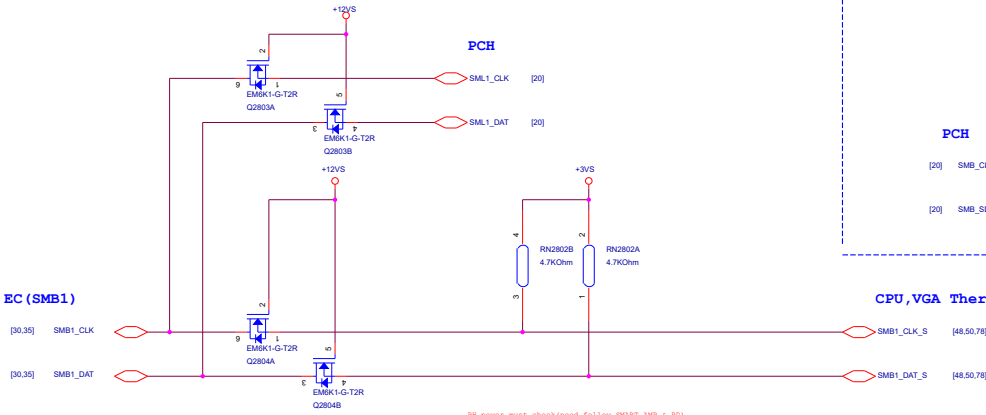
1st: 05006-00090900 FLASH MXIC MX25L12873FM2I-10G 128M SOP-8L
2nd: 05006-00093100 FLASH GD25B127DSIGG IGADEVICE 128MB SOP8


Main Board



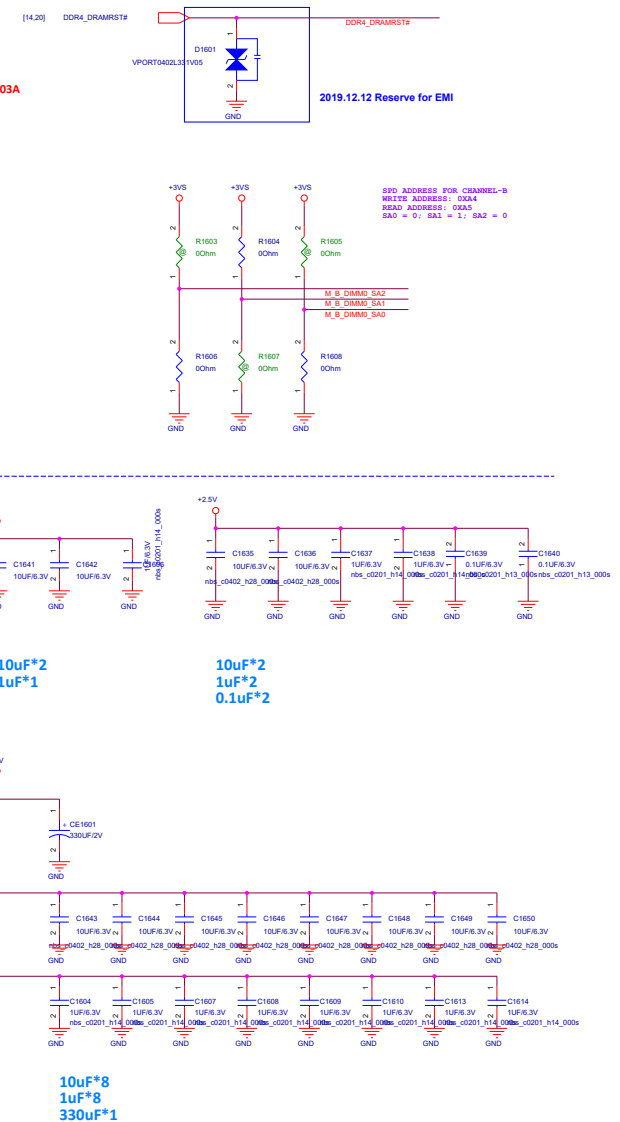
System Management Interface

SMBus Interface




		Project Name	Rev
		GX550LXS	R1.0
Title : TEST POINT			
Size B	Dept.: ASUSTeK COMPUTER	Engineer:	EE
Date: Wednesday, February 19, 2020		Sheet	29 of 103

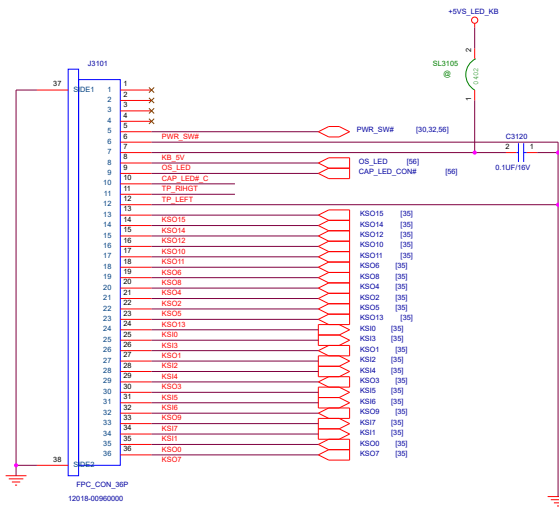
Main Board



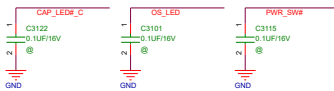
DDR4 - 2666MHz (8G)
1st : Hynix - 03A08-00051800
2nd : Samsung - 03A08-00051700
DDR4 - 2666MHz (16G)
1st : Hynix - 03A08-00061900
2nd : Samsung - 03A08-00061800

		Project Name GX550LXS		Rev R1.0
Title : DIM_DDR4 S0-DIMM B1				
Size C	Dept.: ASUSTeK COMPUTER INC. Engineer: EE			
Date: Wednesday, February 19, 2020			Sheet 16	of 103

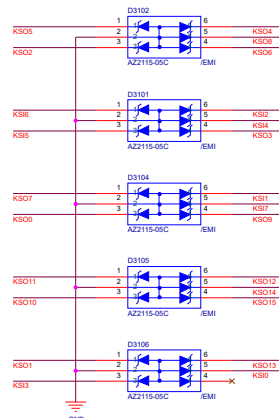
Keyboard Connector



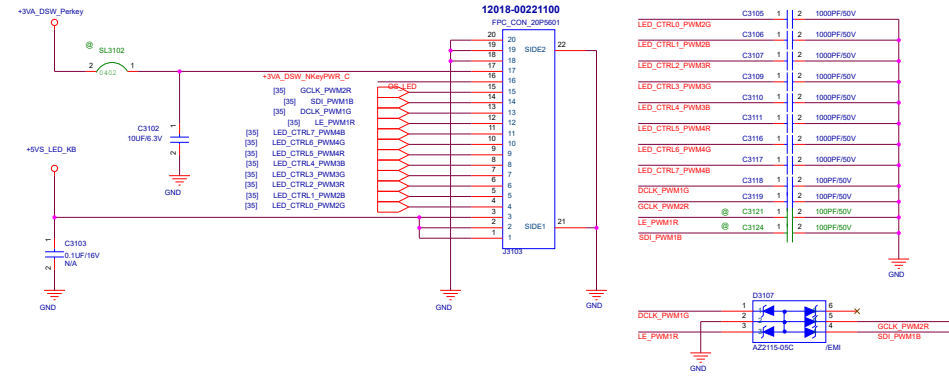
Reserved for EMI



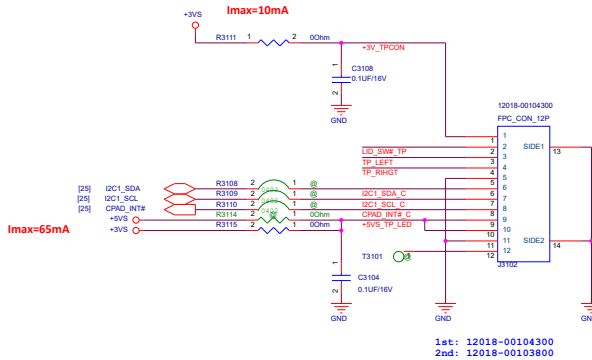
For EMI



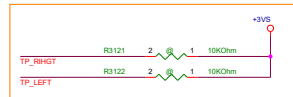
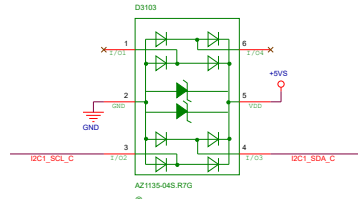
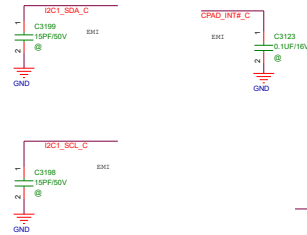
Keyboard LED



Touch Pad / Ten Keys Connector



Reserved for EMI



GX501GE R1.0 2017.07.25

2018/01/04 for EMI Reserved

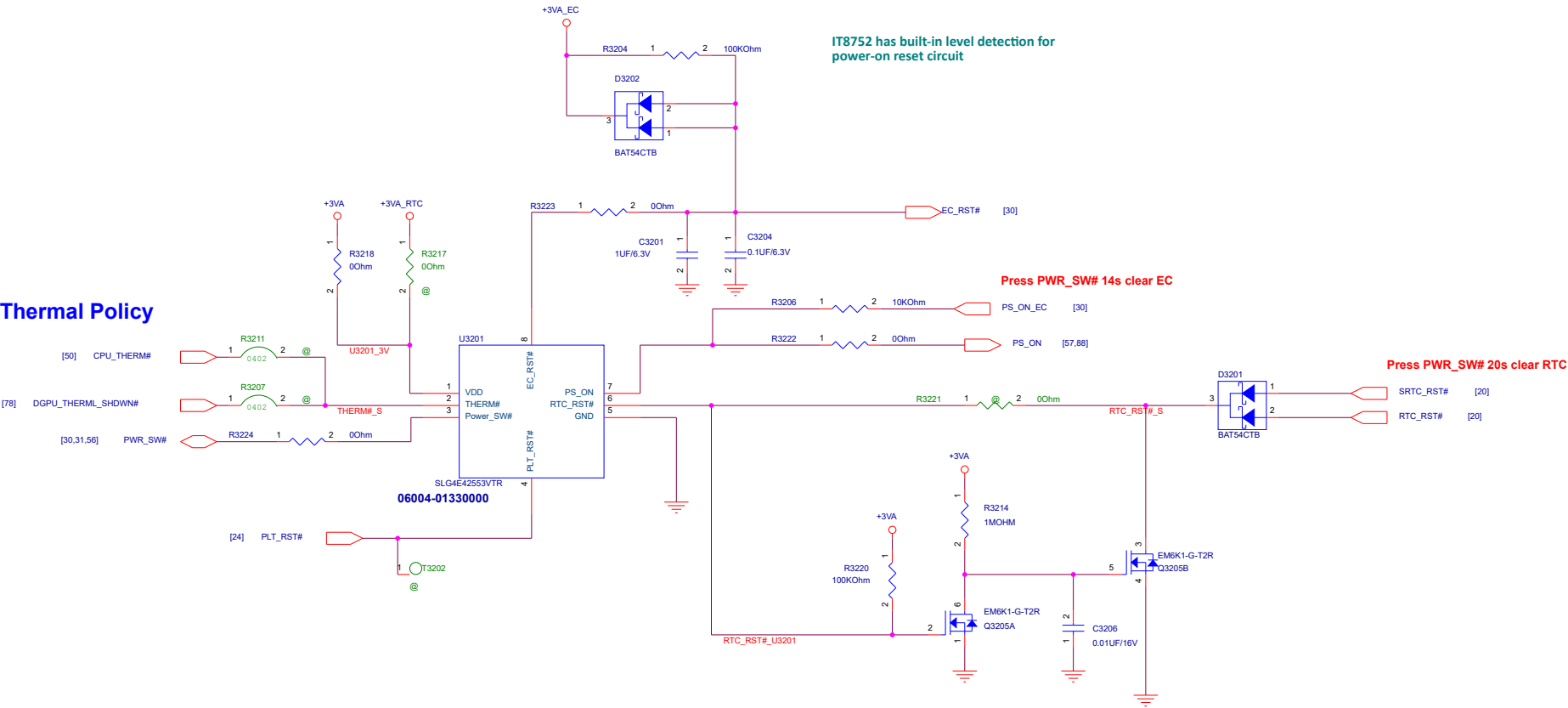
Touch Pad Pin Define

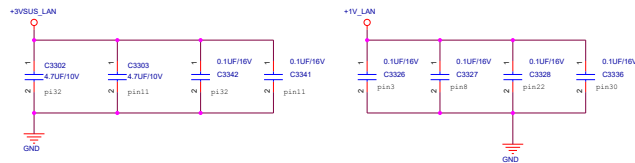
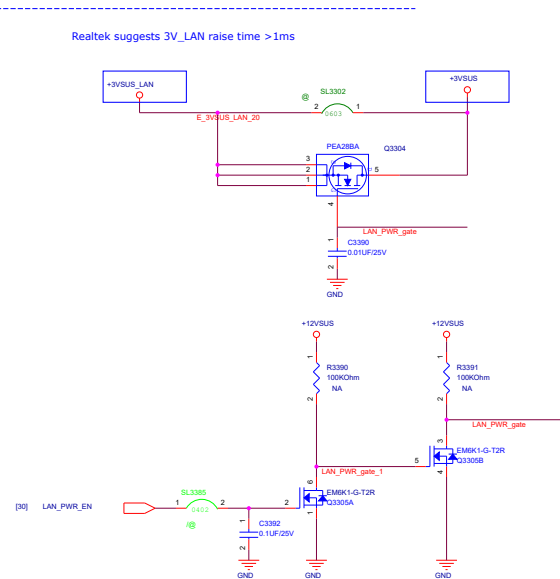
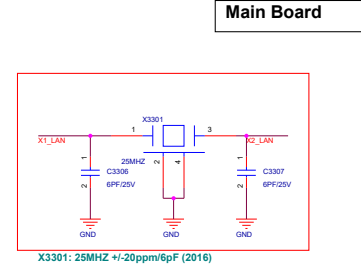
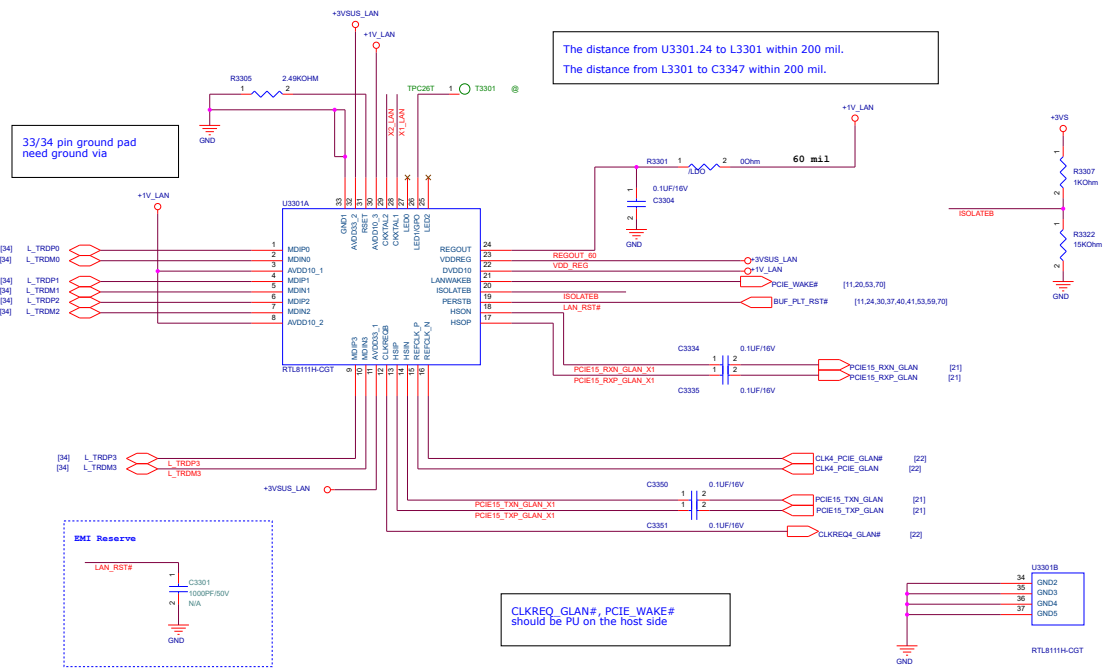
Connector type: 12 pins FFC connector, pitch is 0.5 mm.

Pin#	Signal	I/O	Description
1	VDD_3.3V	Power	3.3V +/-5%. Power ripple: 100 mV/pp max. Power sequence: See section 4.6.
2	LID_CLOSE	I	Lid close/open pin. Indicates that the lid is closed or opened. High when lid is opened. Low when lid is closed.
3	SWL	I	Low active, left button signal.
4	SWR	I	Low active, right button signal.
5	GND	GND	Ground
6	SDA	I/O	I2C data. I/OV of I2C: 8 mA max.
7	SCL	I/O	I2C clock. I/OV of I2C: 8 mA max.
8	INT	O	Active low, indicates that the touchpad plans to send data to host
9	LED_VDD	Power	Power for LED circuit. 3.3V, driver current: TBD
10	LED_VDD	Power	Power for LED circuit. 3.3V, driver current: TBD
11	GND	GND	Ground
12	LED_CONTROL	I	To lighten the LED when high. High active

<Core Design>

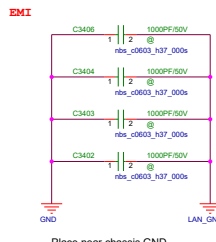
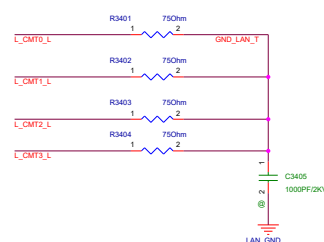
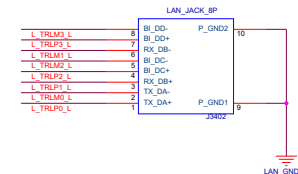
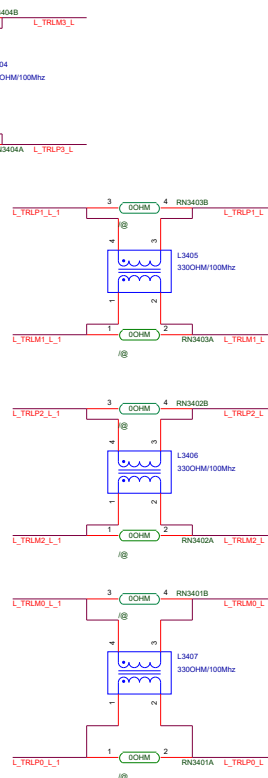
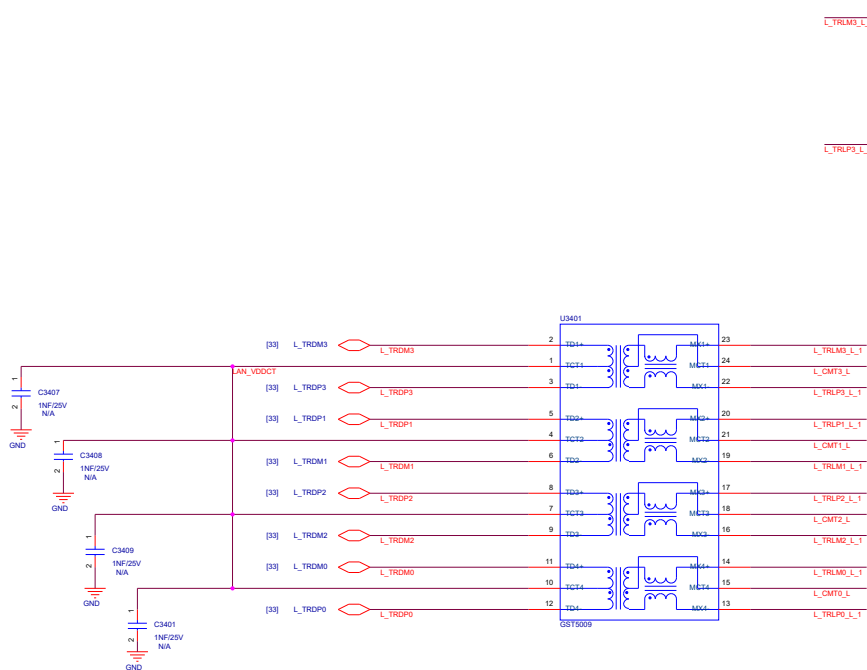
Thermal Policy



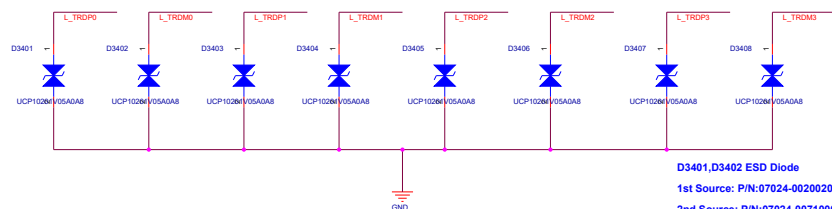


Main Board

LAN Connector



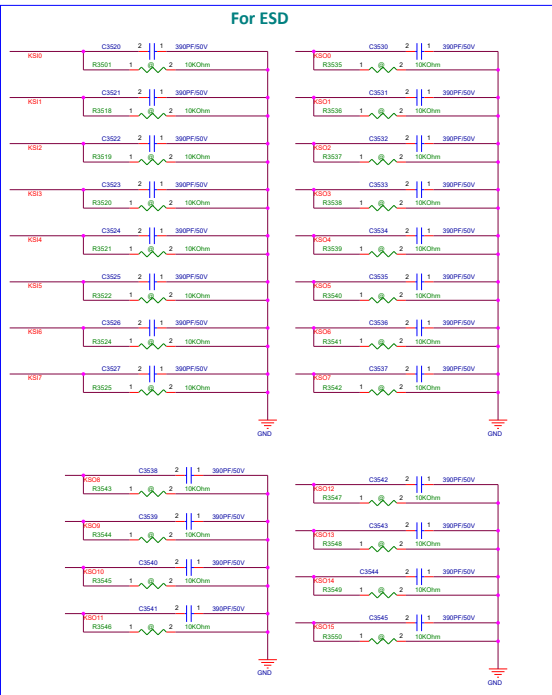
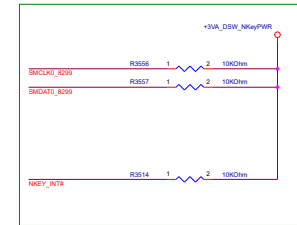
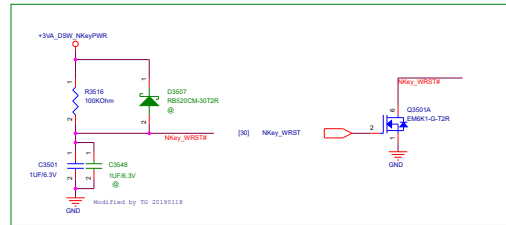
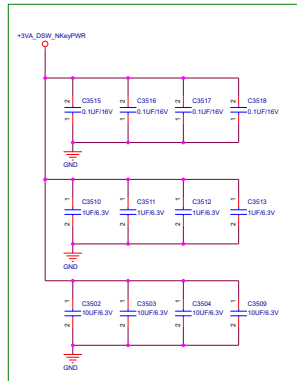
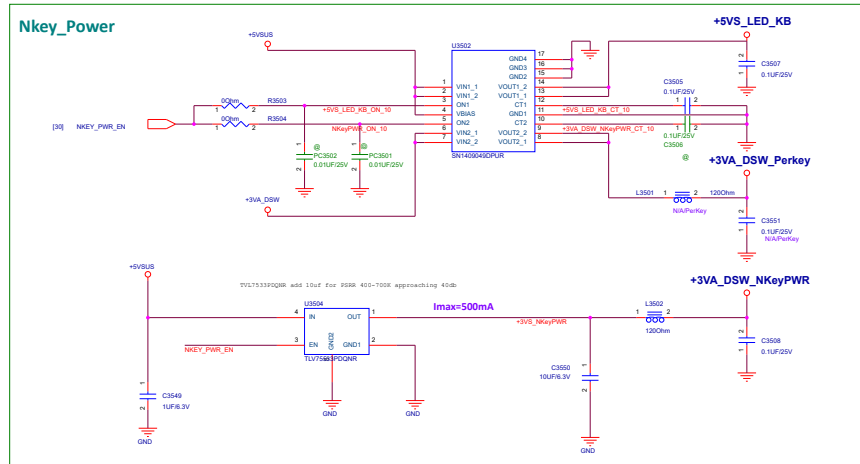
GND_LAN_T 上禁止加任何零件



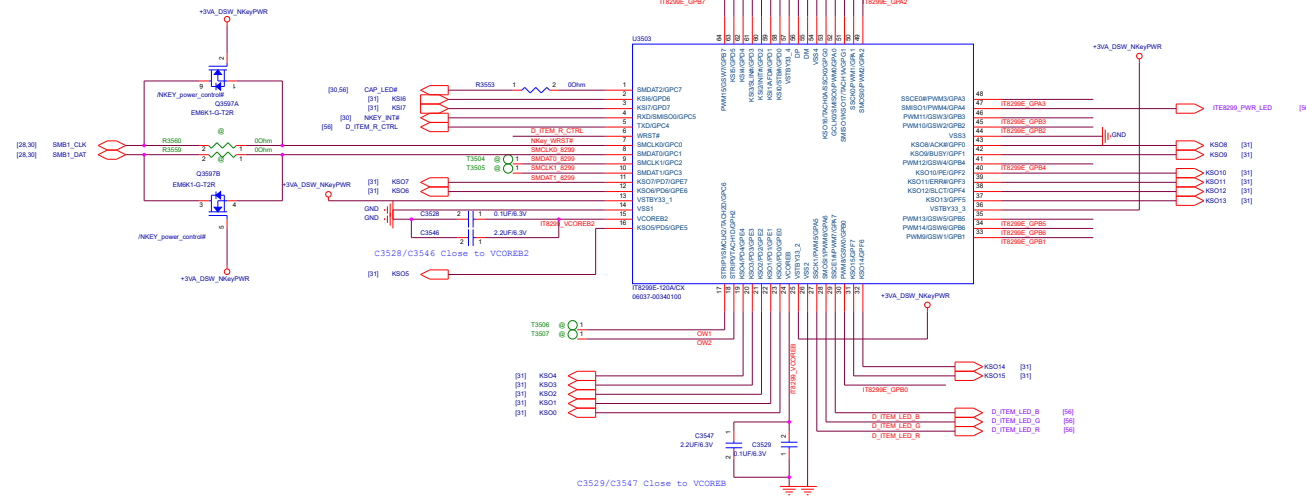
D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

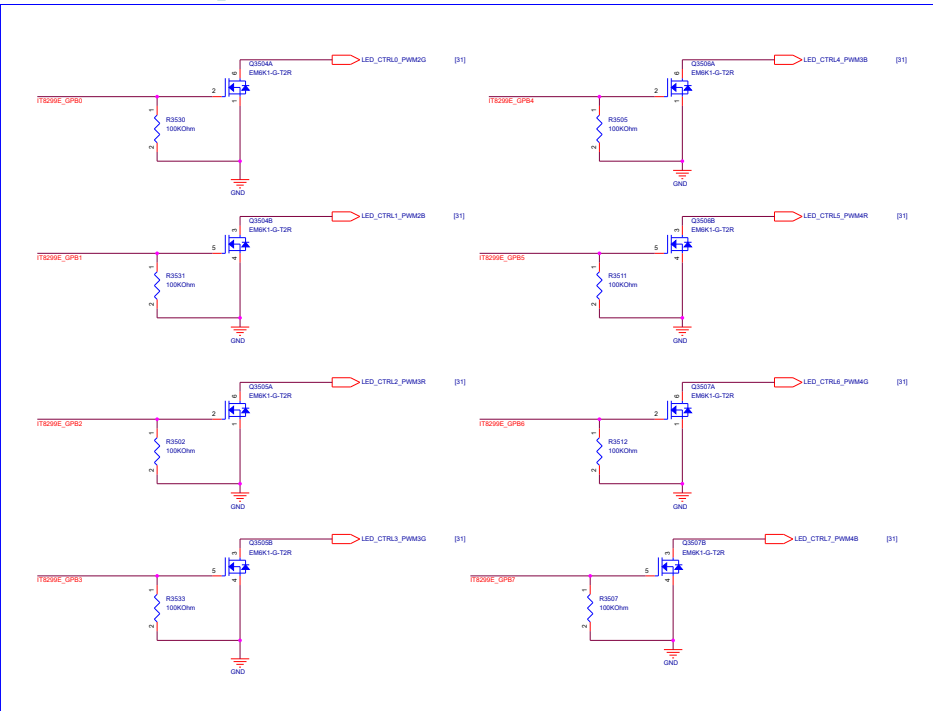
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



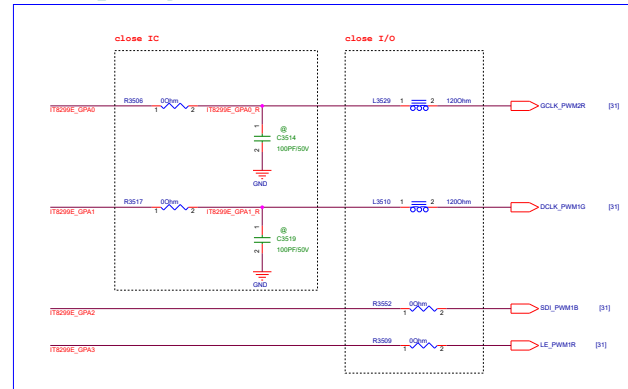
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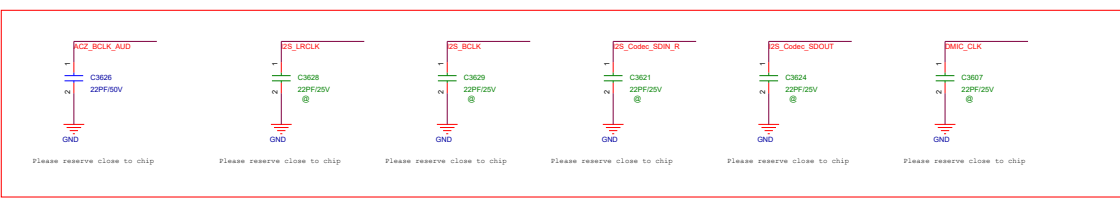
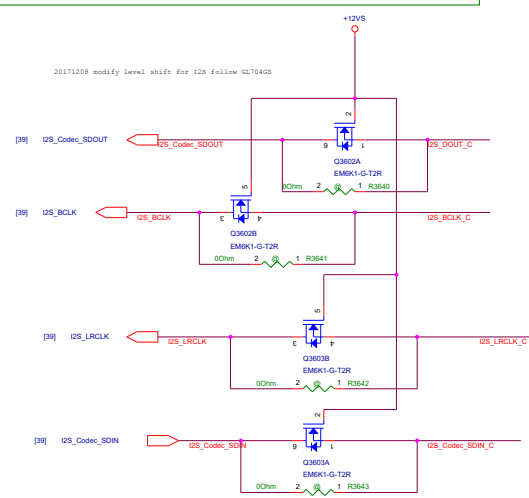
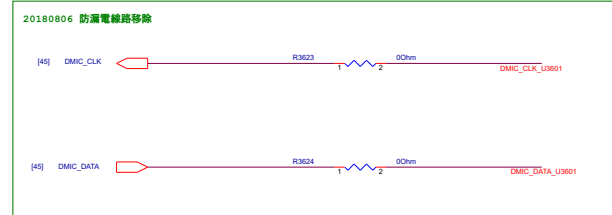
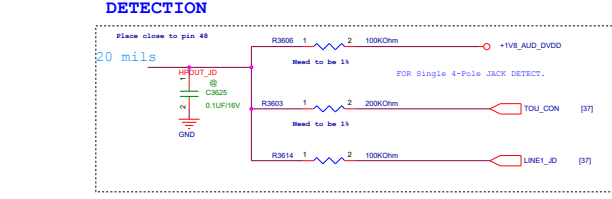
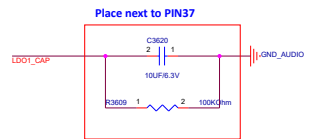
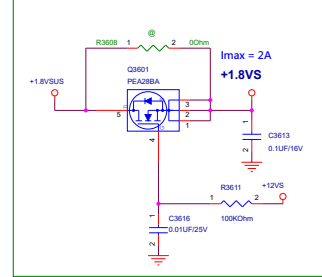


KB RGB Per Key LED



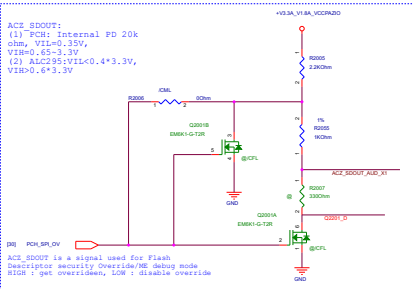
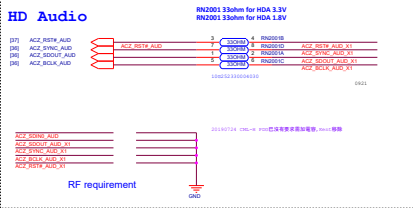
PerKey Signal



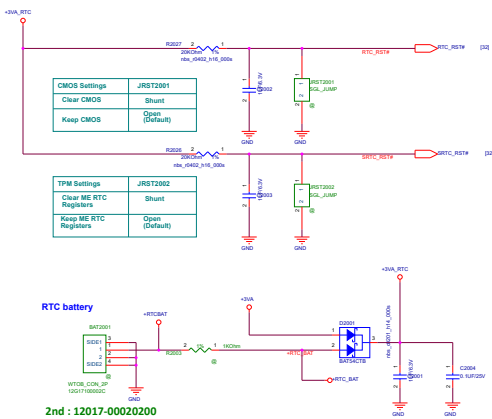


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HD Audio



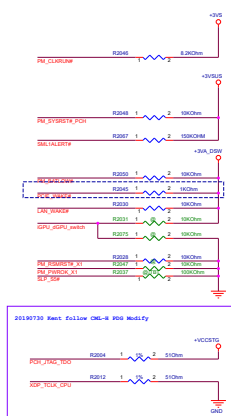
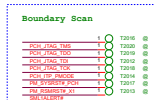
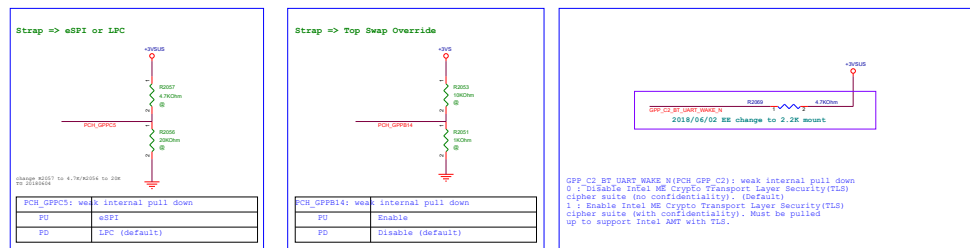
Main Source	1th FWR	2nd FWR	3rd FWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.05VSUS	+VCCST		
	+1.2V			
	+3VAO	+3VA	+3VA_EC	
	+3VA_DOW	+3VSUS	+3VSUS_PCH	
		+3VS		



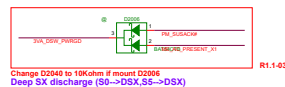
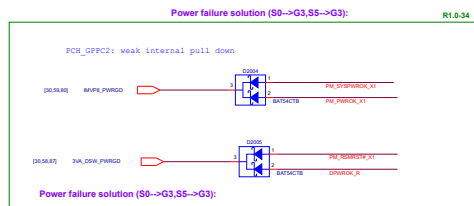
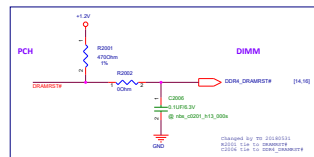
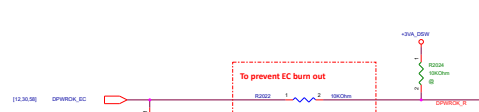
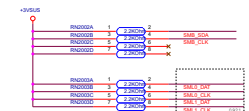
USE RTC Battery:
P/N: 0B100-00040500 BATT-LI CR1220 3V

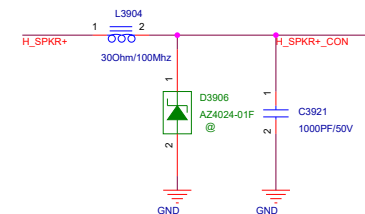
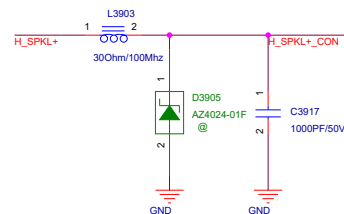
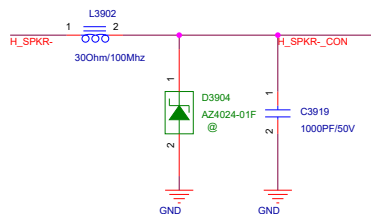
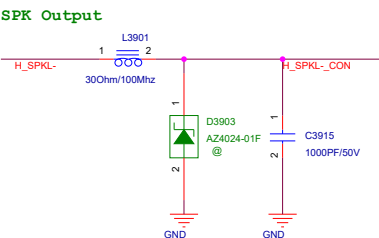
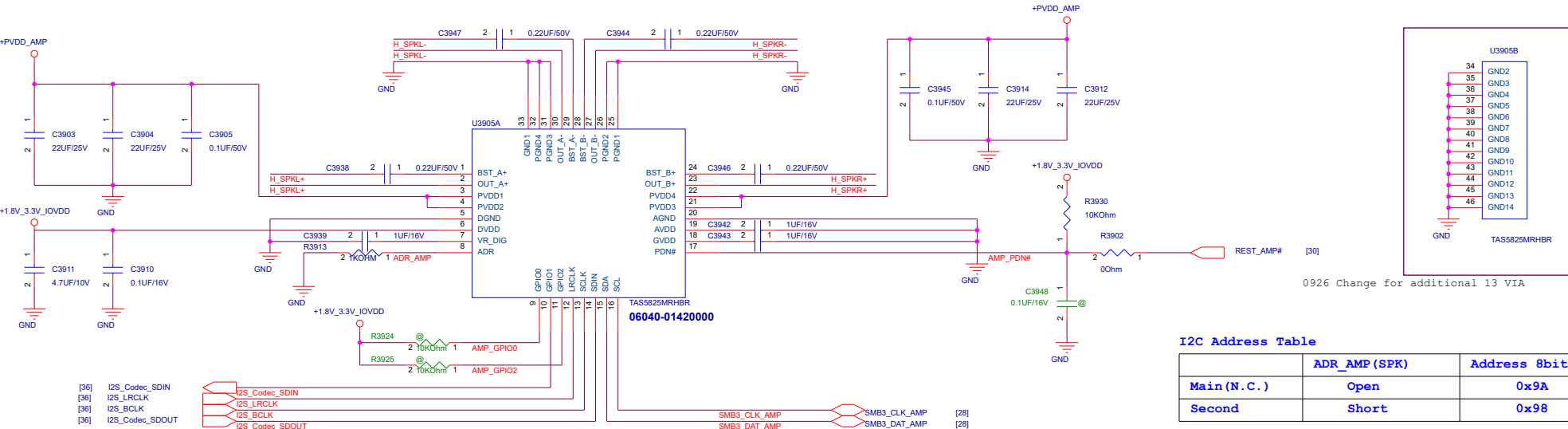
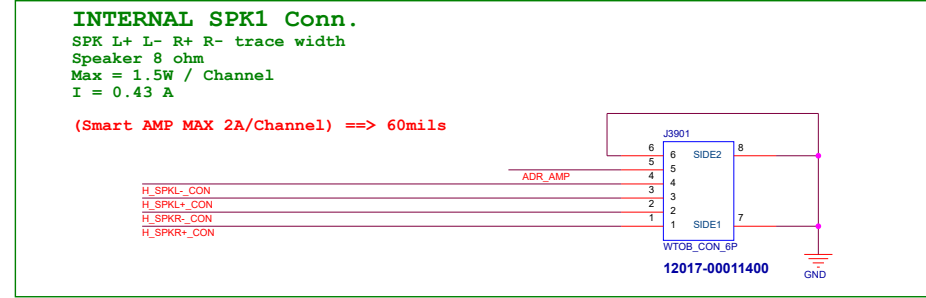
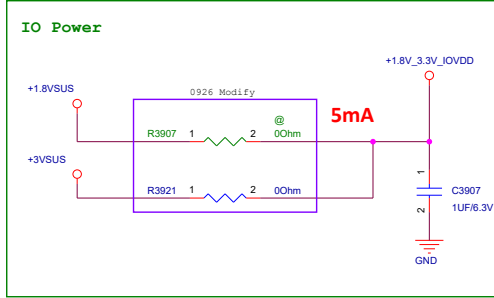
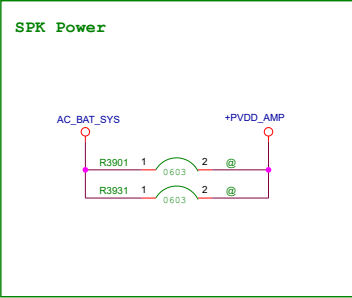


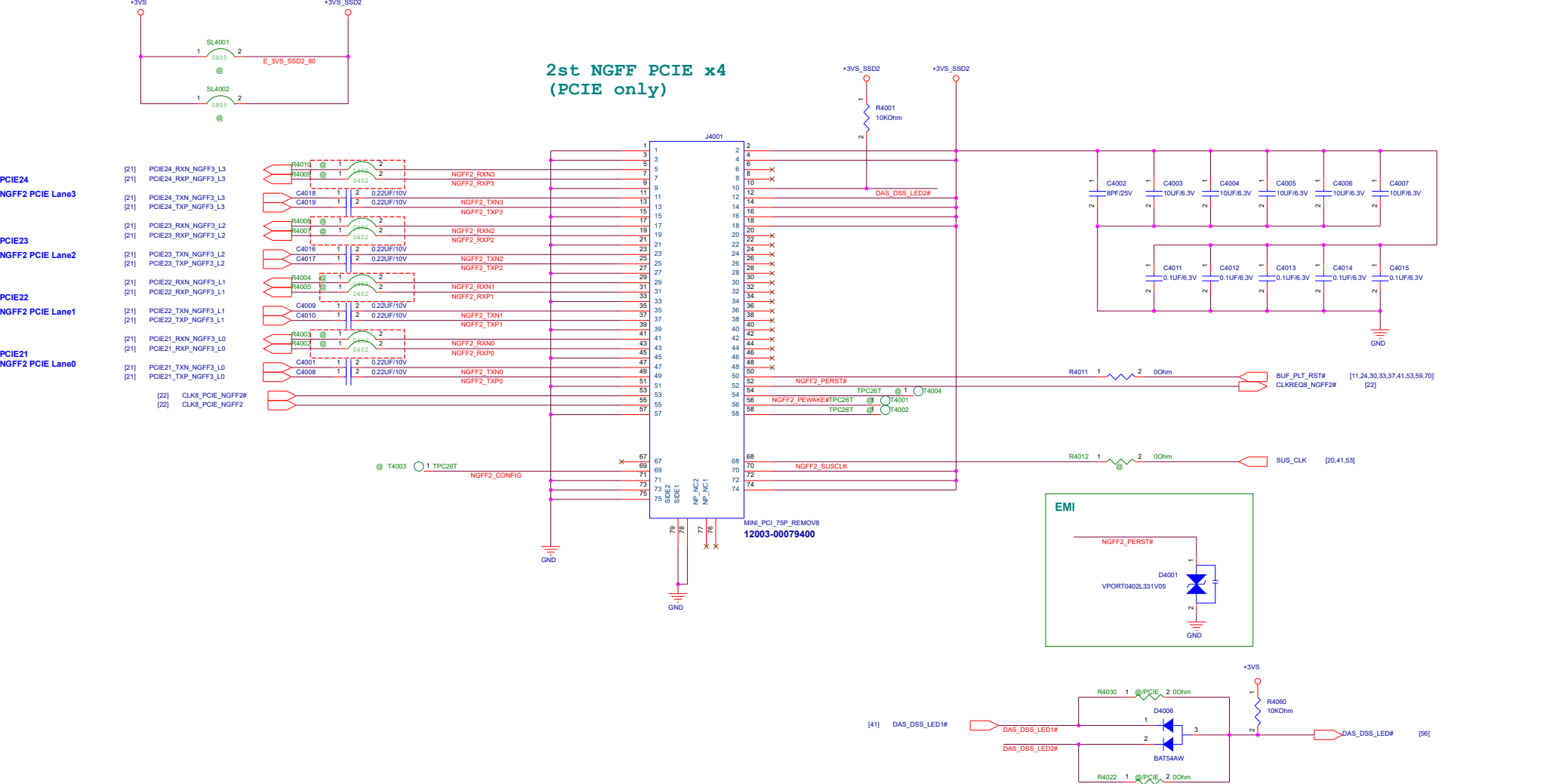
Power failure solution (S0-->G3,S5-->G3):



SMBUS









Project Name

GX550LXS

Rev

R1.0

Title : **CR_GL9750 colay GL9760**

Size

C

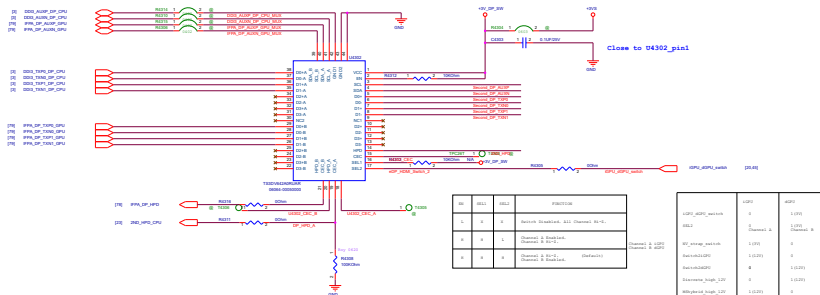
Dept.: **ASUSTeK COMPUTER INC. NB1** **Engineer:** **EE1_RD TG_Wei**

Date: **Wednesday, February 19, 2020**

Sheet **42** of **103**

Second Display Switch

DP Switch

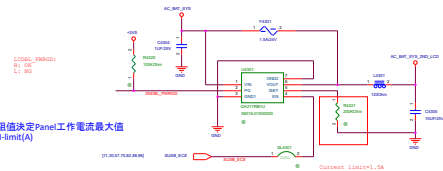


LCD Power switch

Power Switch IC Protection Circuit

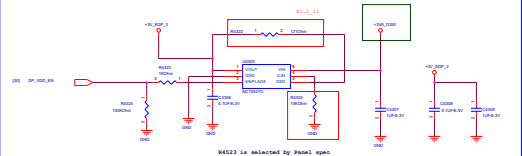
180423 Holton
Add Power Switch circuit with GA217 06016-01930000

Mark Copy UX461FN 1129

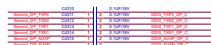


※R_iset (R4541)的阻值決定Panel工作電流最大值
 $R_{iset}(Kohm) = 300 / I_{-limit}(A)$

LCD Power switch

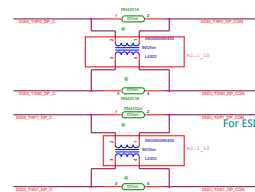


2nd Display

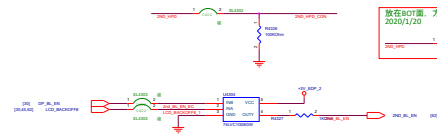
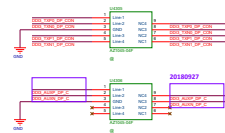


Mark Connection need to check 1123

10.3



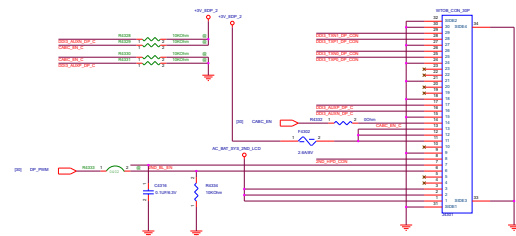
For ESD



放在BOT圖。方便debug
2020/1/20

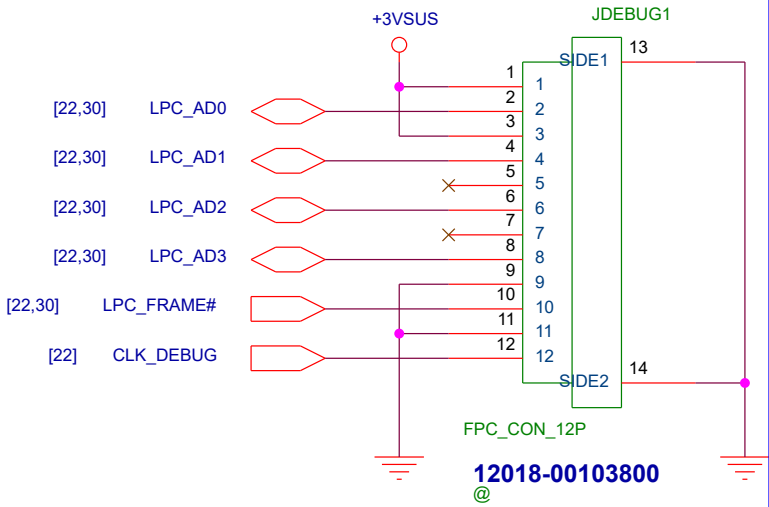
1

Mark need to Check with WC 1211



LPC Debug Port

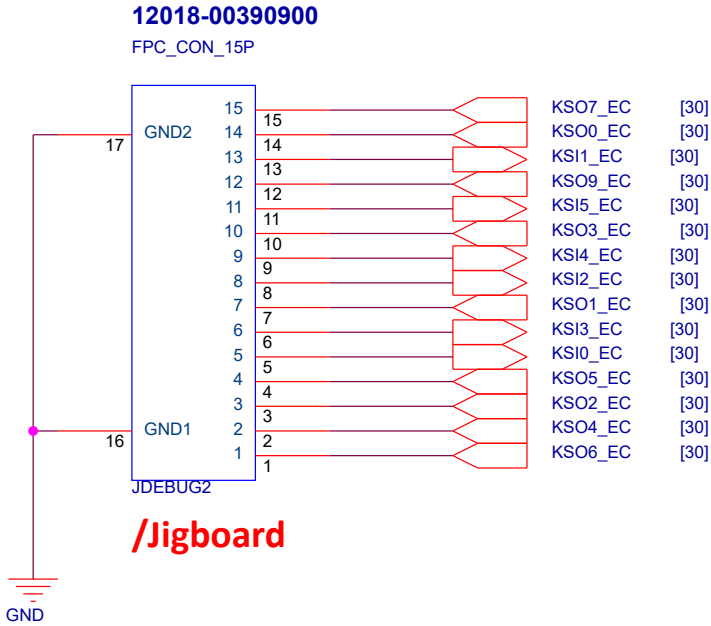
2017/11/10




1st: 12018-00103800
2nd :12018-00103300

2017/11/10


Flash BIOS




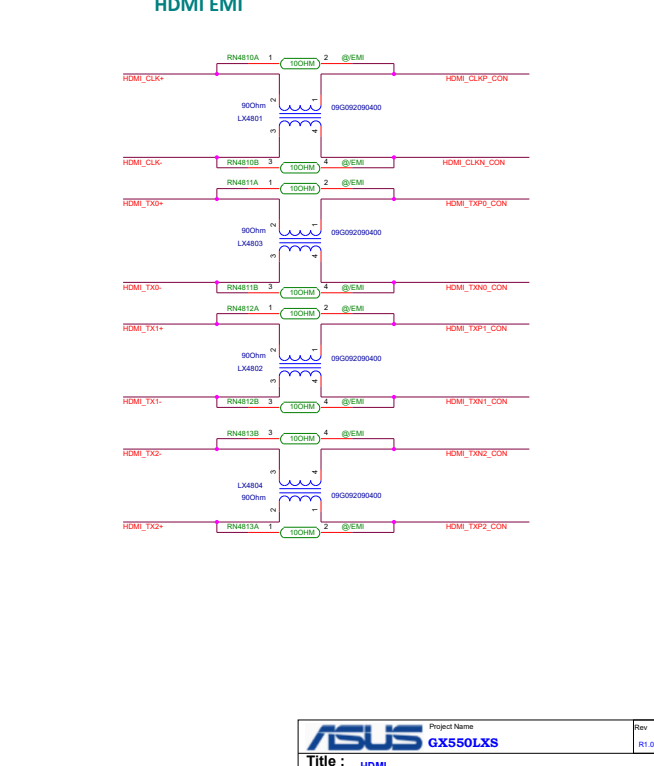
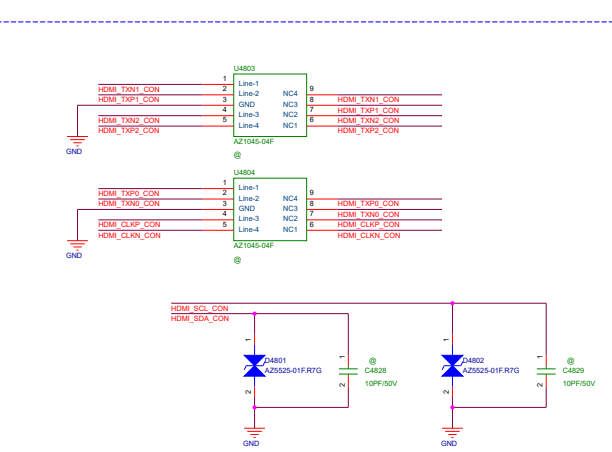
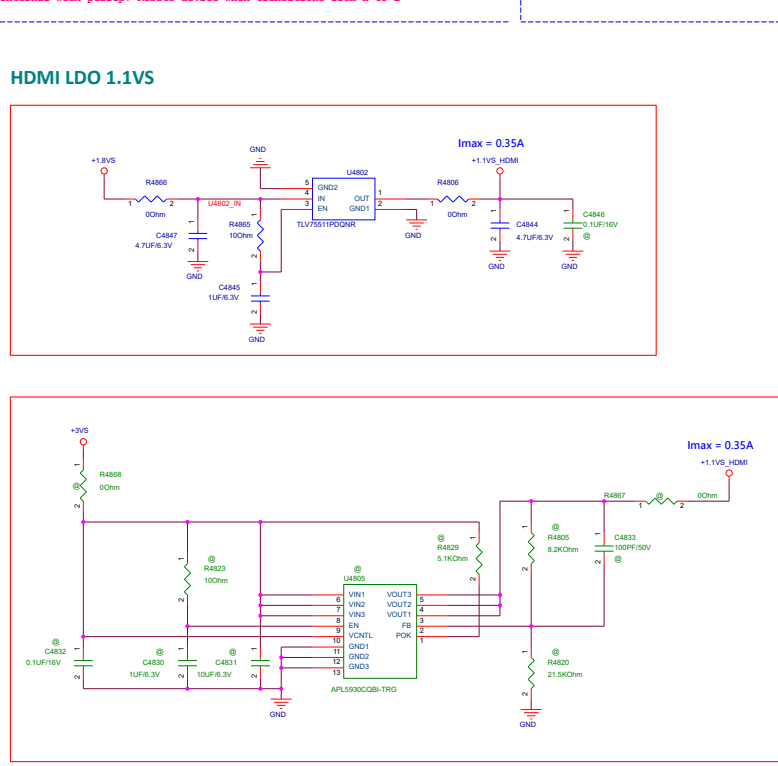
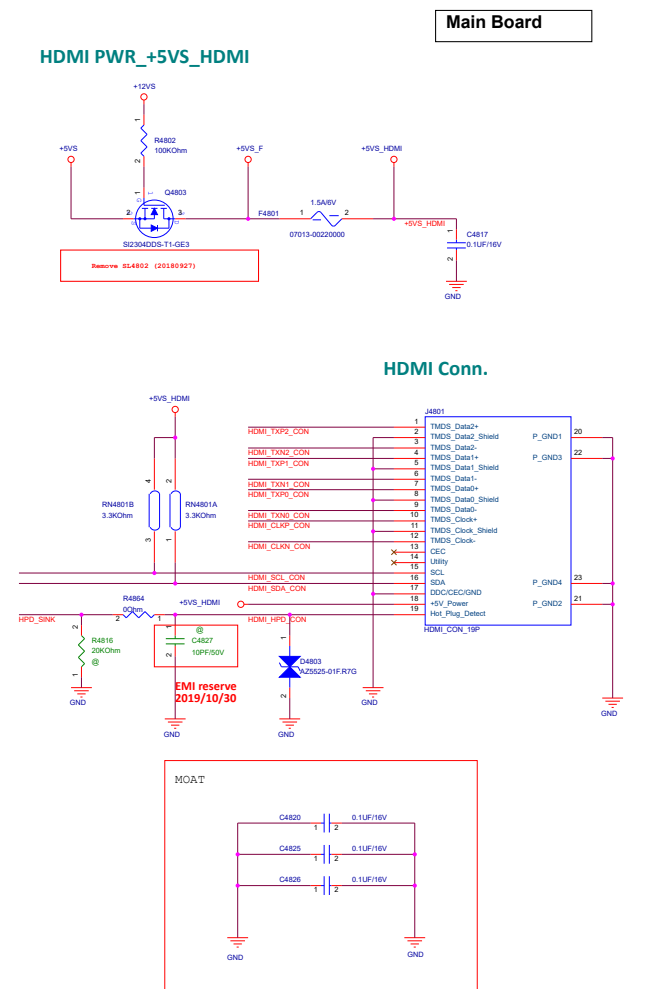
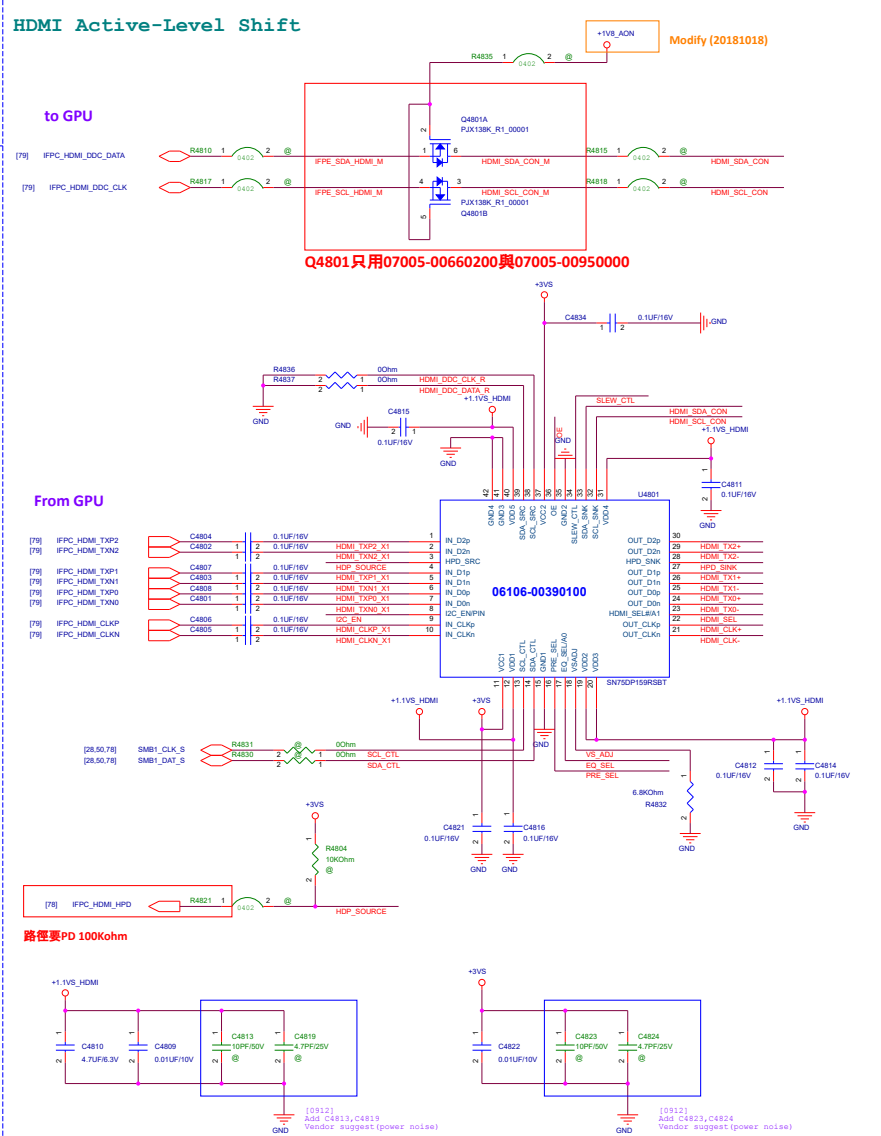
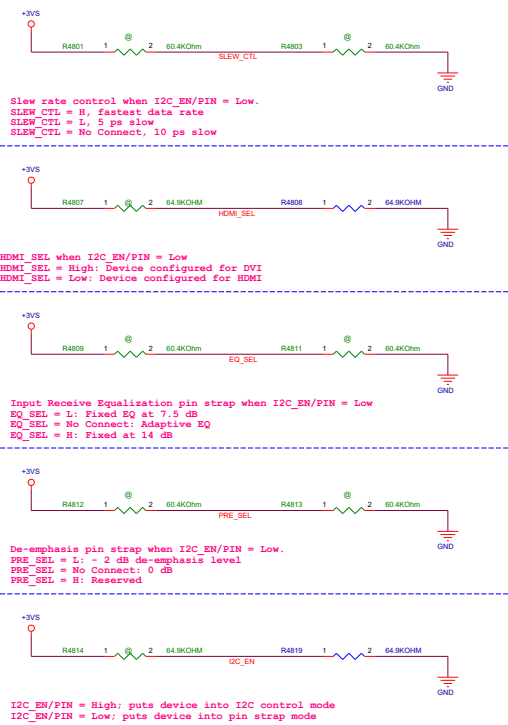
<Core Design>

		Title : DEBUG_LPC	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX550LXS		Rev R1.0
Date: Wednesday, February 19, 2020		Sheet 44 of 103	

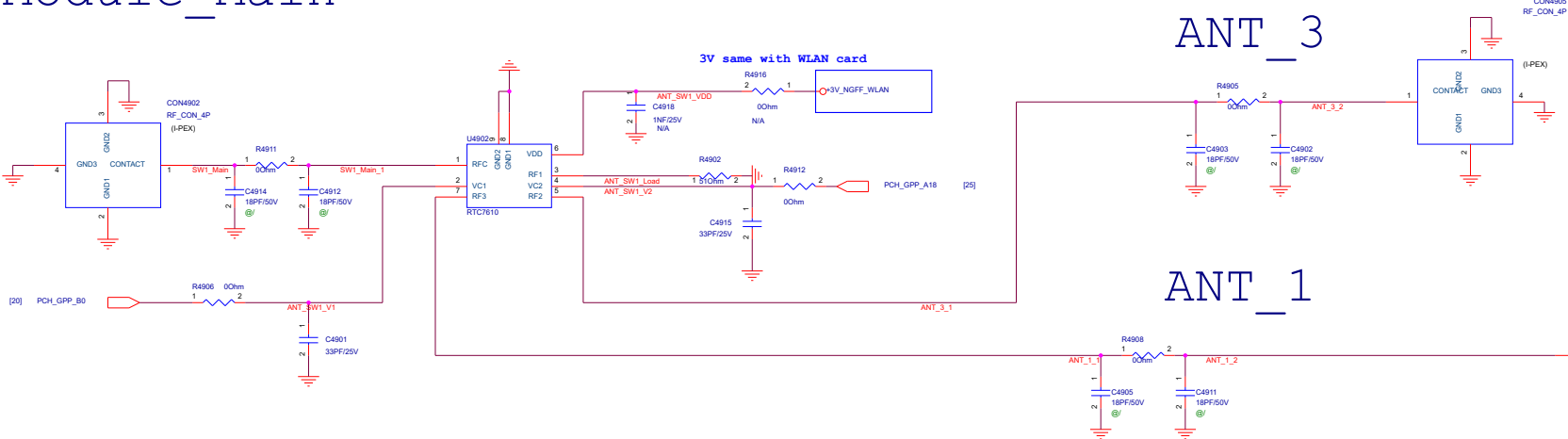
<Variant Name>

		Project Name		Rev	
		GX550LXS		R1.0	
Title : CRT_eDP					
Size Custom	Dept.: ASUSTeK COMPUTER		Engineer:	Mario_Jhu	
Date: Wednesday, February 19, 2020			Sheet	46	of 103

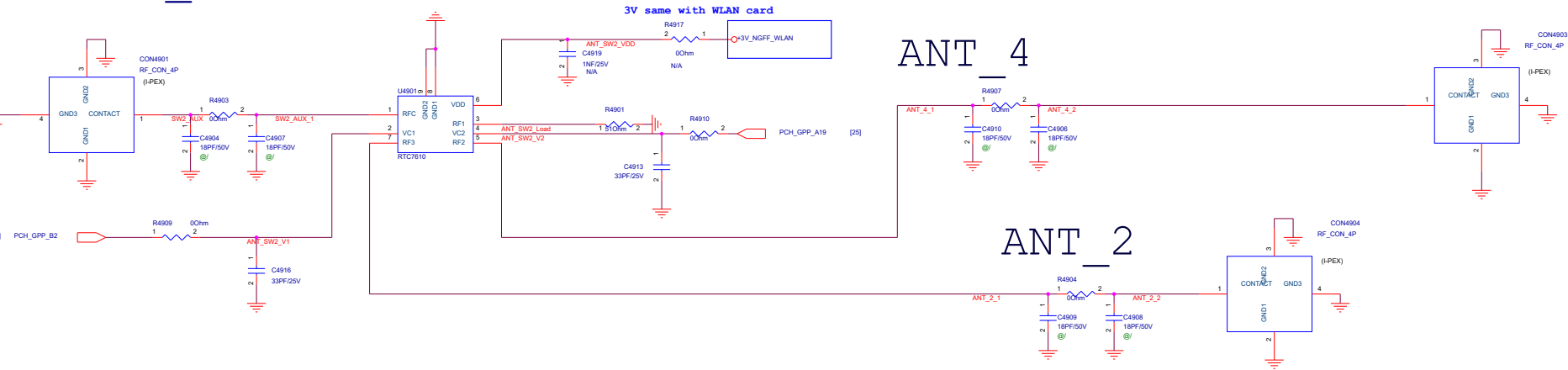
		Title : TYPE-C USB3.1_R1.5_4	
ASUSTeK COMPUTER INC. NB1		Engineer:	
Size	Project Name		Rev
D	GX550LXS		R1.0
Date:	Wednesday, February 19, 2020	Sheet	47 of 103



Module_Main



Module_AUX



U4901 RTC7610				
AUX		V1	V2	V3
ANT	Port	GFP_B2	GFP_A19	
ANT_4	RF1			
ANT_2	RF2			
50 Ω	RF3			

U4902 RTC7610				
Main		V1	V2	V3
ANT	Port	GFP_B0	GFP_A18	
ANT_3	RF1			
ANT_1	RF2			
50 Ω	RF3			

0: 0 v ~ 0.3v
1: 3 v ~ 3.6v

<Core Design>

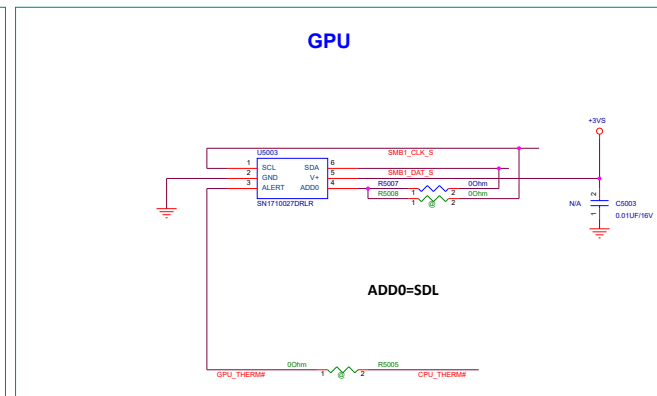
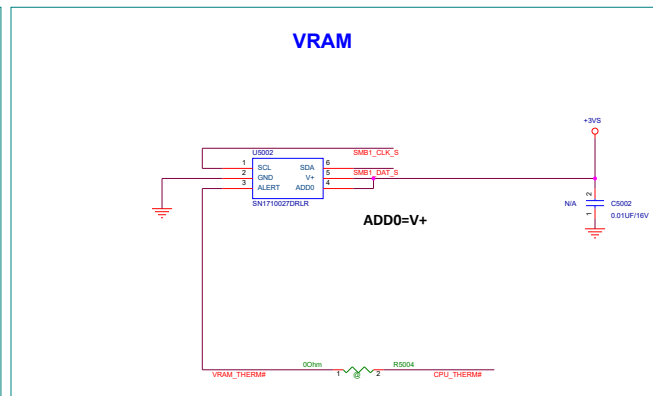
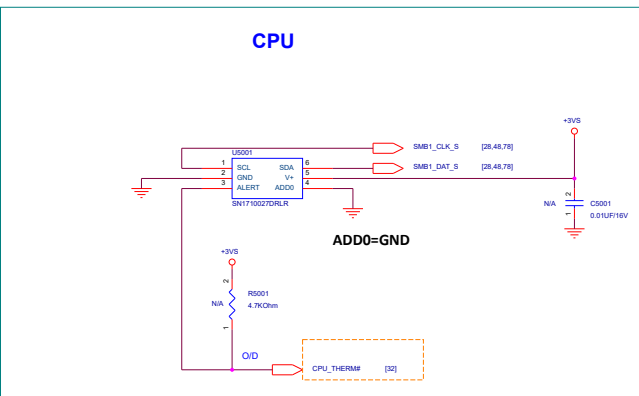
Thermal Sensor : SN170027

ALERT/SDA/SCL: Open-drain output; pullup resistor 5Kohm

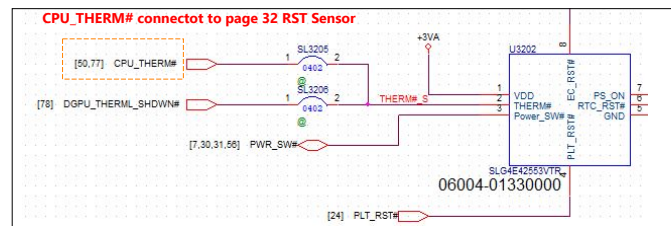
Pin function Supply voltage:- 1.62 V to 3.6 V

power rail : 3.3V

SMBUS1 to EC

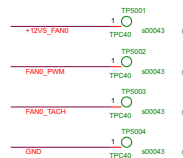
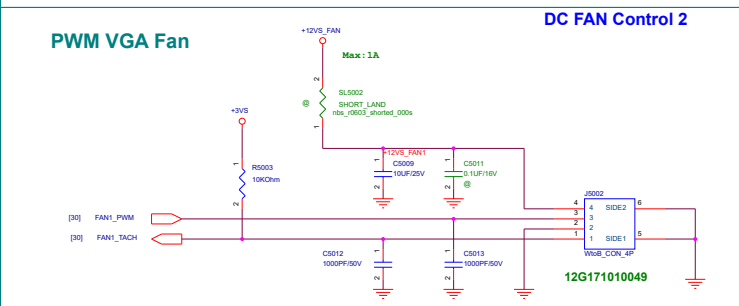
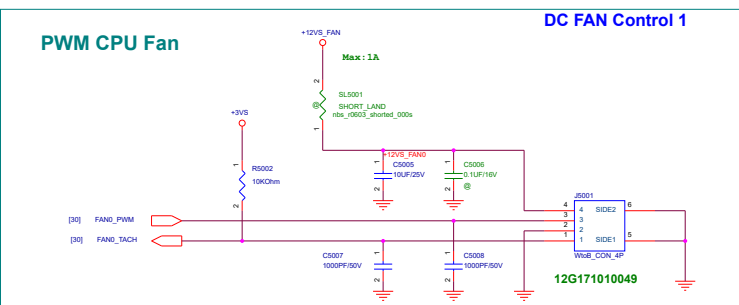


example



ADD0: Address select. Connect to GND, SDA, SCL, or V+

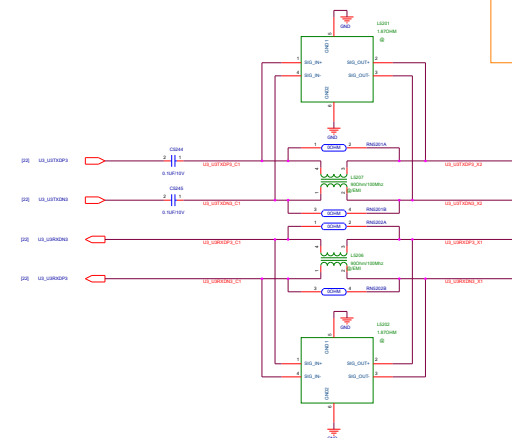
DEVICE TWO-WIRE ADDRESS	ADD0 PIN CONNECTION	Output
100100090	Ground	CPU
100100191	V+	VRAM
100101092	SDA	GPU
100101193	SCL	



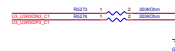
©Core Designer

USB3.1_Port3 (Gen2)

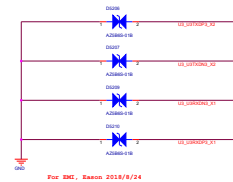
USB3.0 EMI-Protection



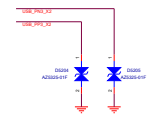
Short Protection



USB3.0 ESD-Protection



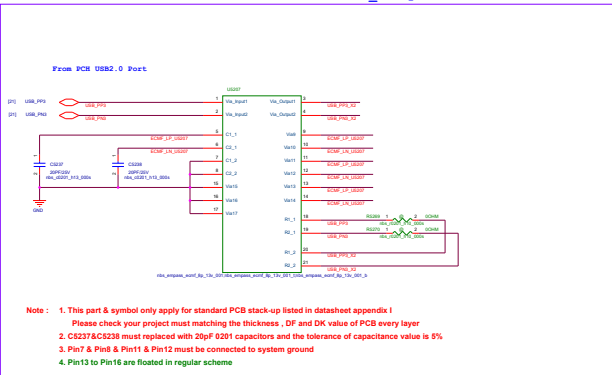
USB2.0 ESD-Protection



2017/11/23 Changed by James
Add U300A/D3305

For SMC, Sann 2016/9/24

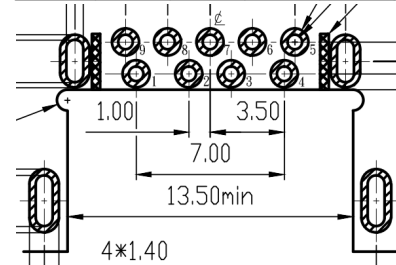
USB2.0 EMI-Protection With ECMF(PCB 1.05mm_12Layer)



temp_M08_000007層名順序是 : TOP/GND/IN1/GND1/IN2/VCC/VCC1/IN3/GND2/IN4/GND3/BOTTOM

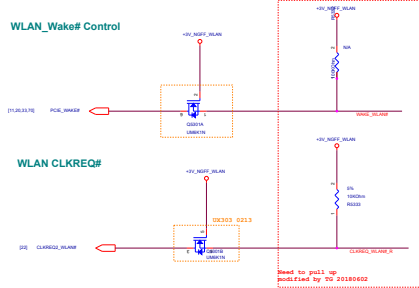
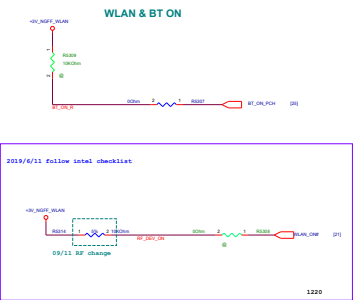
5.PIN DEFINE TABLE:

PIN NO.	1	2	3	4		
SIGNAL NAME	VBUS	D-	D+	GND		
PIN NO.	5	6	7	8	9	
SIGNAL NAME	St dA_SSRX-	St dA_SSRX+	GND-DRAIN	St dA_SSTX-	St dA_SSTX+	



(Units: mm)

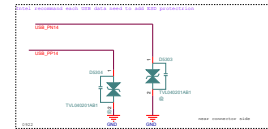
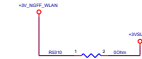
Title : USB Charger	
Revision: 00000000	Engineer: EE
Drawn: 11/23/2017	Check: 11/23/2017
QC: GX50LXS	Rev: 01.0



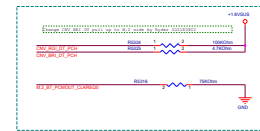
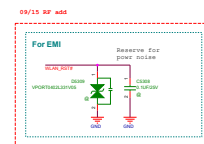
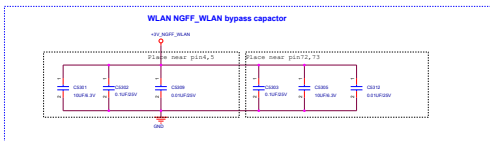
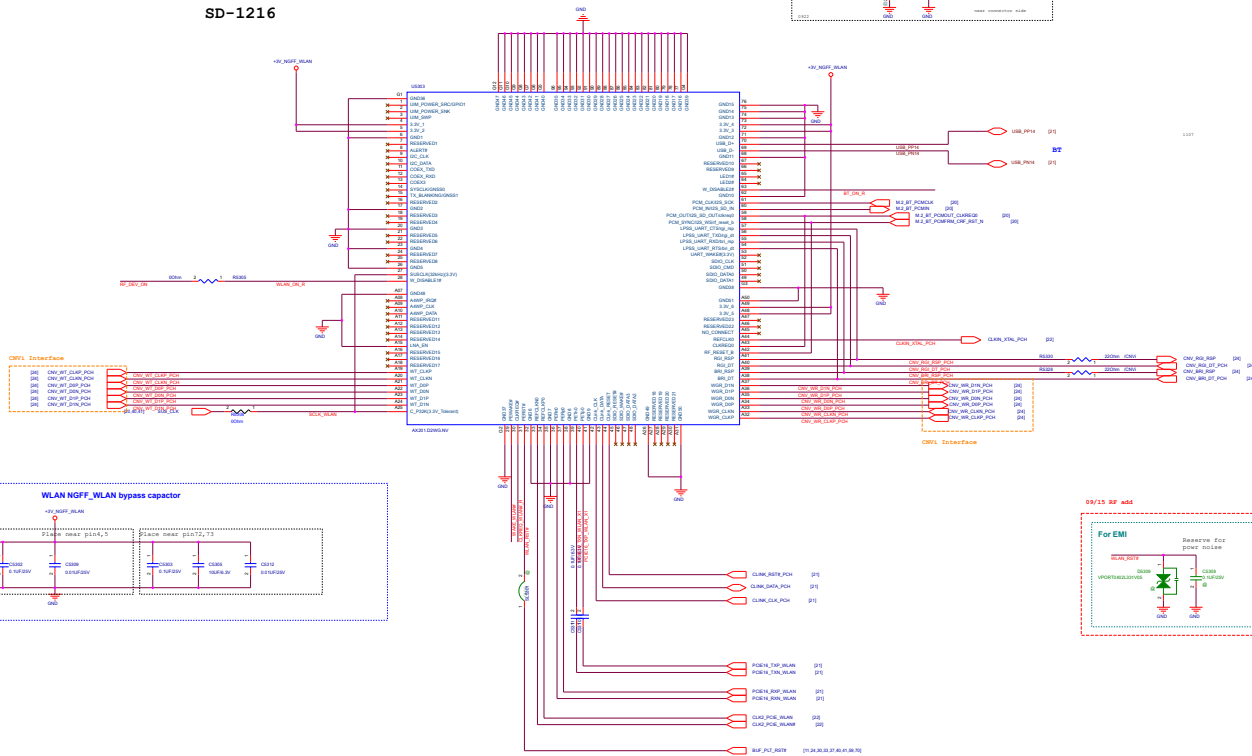
WLAN_PWR_+3V_NGFF_WLAN (Non-15CT)

Support ASUS Open Cloud Computing (ACAccess)

WLAN_PWR_+3V_NGFF_WLAN




SD-1216

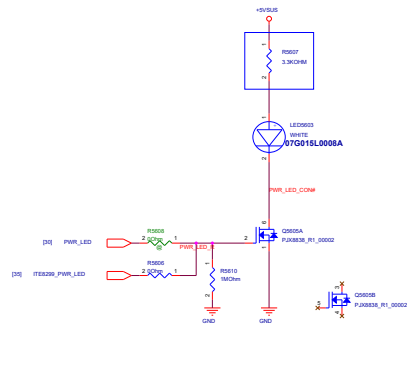


Cloud Design

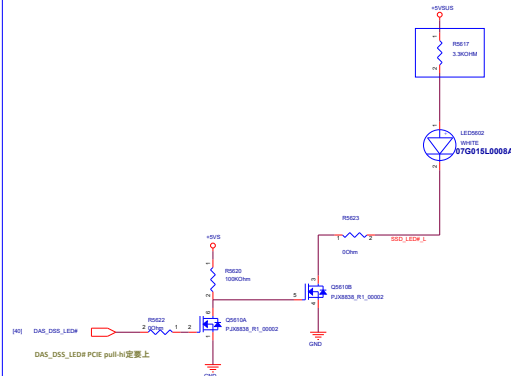
Title <Title>		
Size A	Document Number GX550LXS	Rev R1.0
Date:	Wednesday, February 19, 2020	Sheet 54 of 103

		Title : IO Con. to MB	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX550LXS		Rev R1.0
Date: Wednesday, February 19, 2020		Sheet 55 of 103	

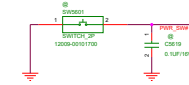
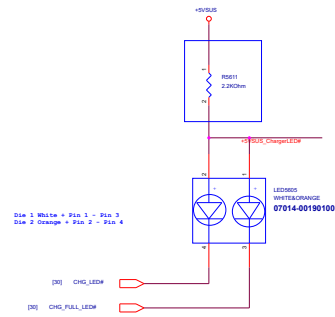
DWR LED



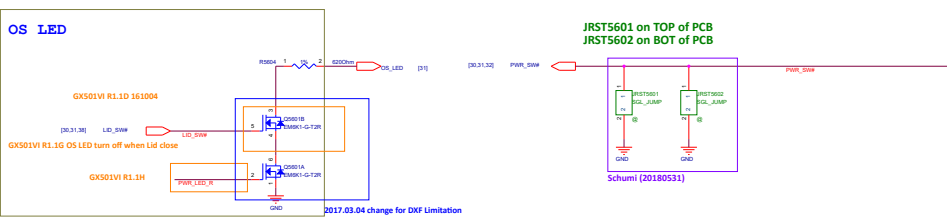
PCIE SSD LED



Charger LED

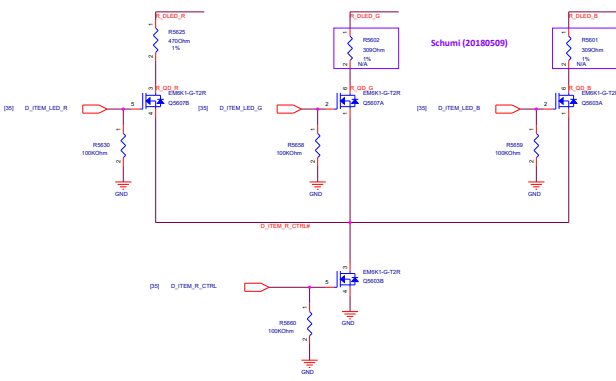


S LED

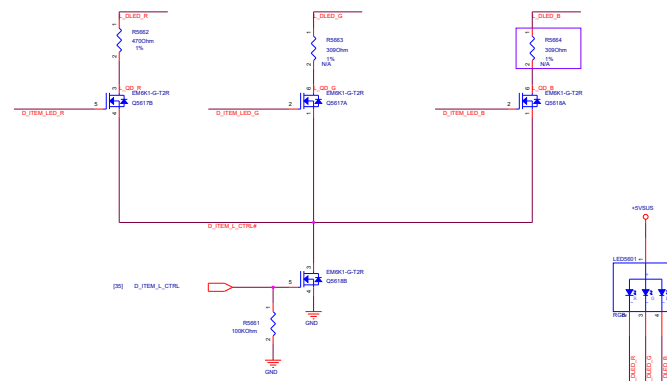


1 Item- RGB LED

< D case LED R >



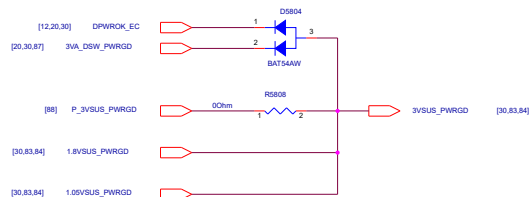
< D case LED L >



CAP LED

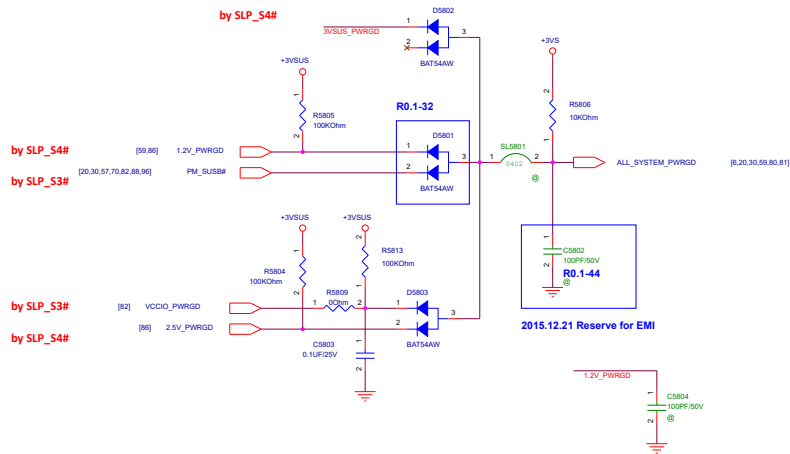


SLP_SUS_N
V0.85_PWRGD
V3.3A_VSA_PWRGD
V1.0A_PWRGD
V1.8A_PWRGD
DPPWRGD=3.3A_DSHPWRGD+10ms & BATT>5.35V

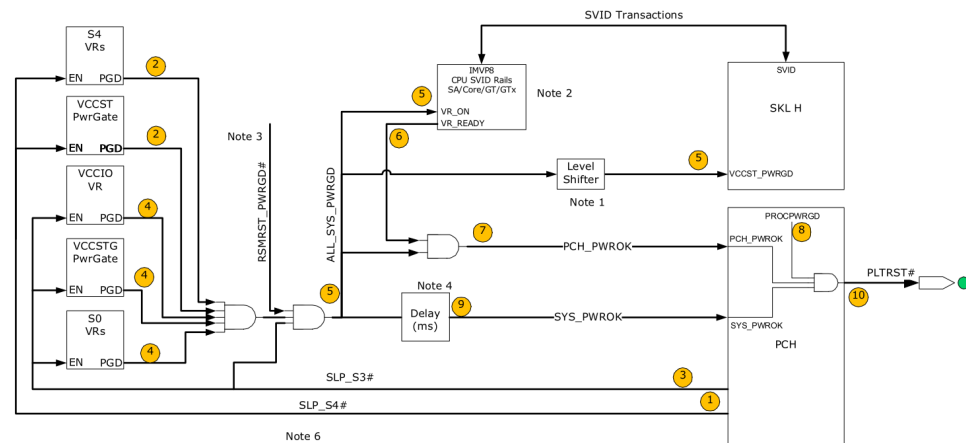
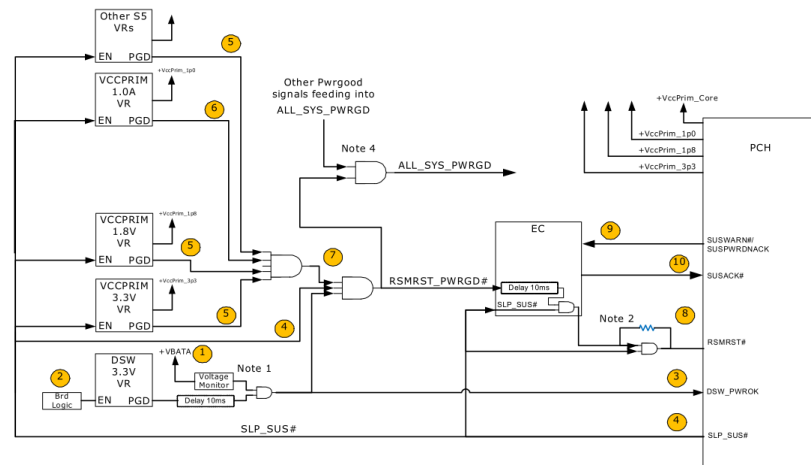
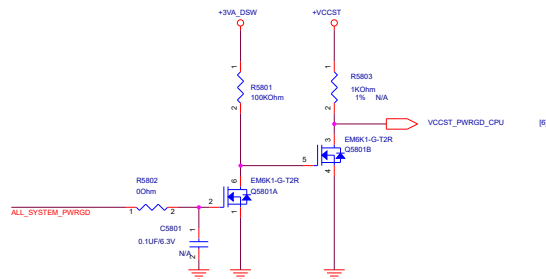


[ALL_SYSTEM_PWRGD]

SLP_S3_N
DDR_PWRGD
VCCIO_PWRGD
3.3S_MON
1.00U_MON
1.8S_MON
RSMRST_PWRGD
SYS_PWROK



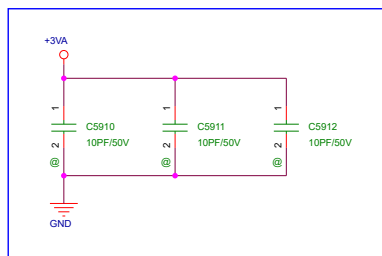
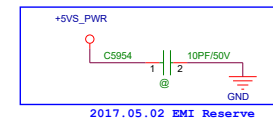
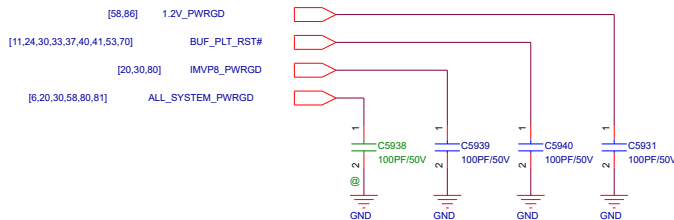
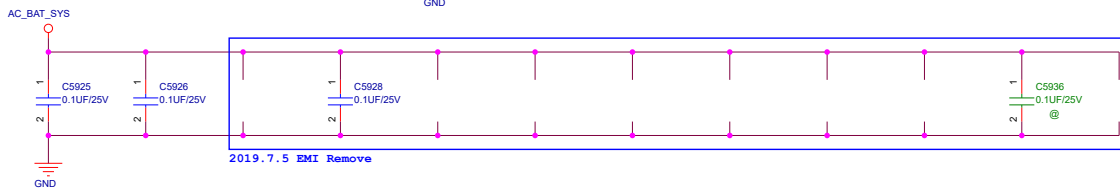
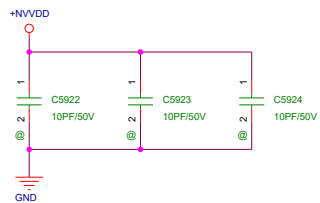
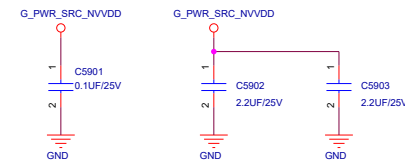
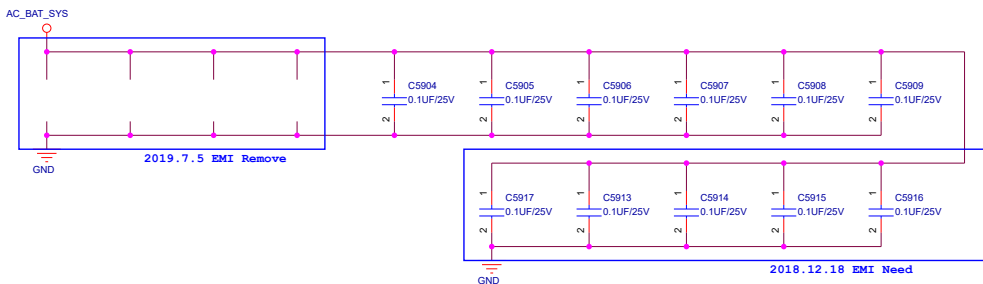
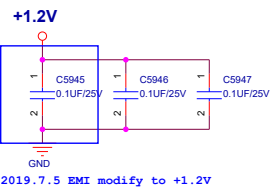
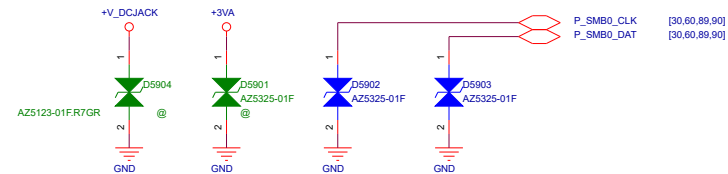
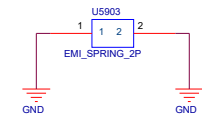
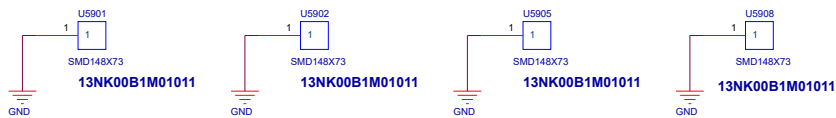
[VCCST_PWRGD for PCH]



<Core Design>

EMI SPRING (4.2H)*4 13NK00B1M01011

ME component list 20190626



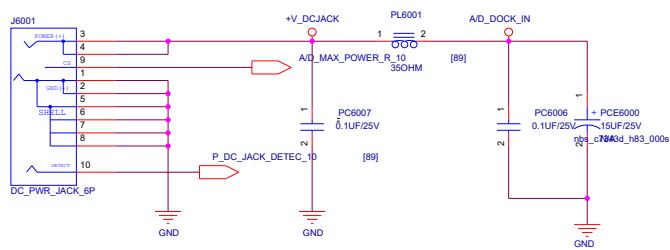
<Core Design>

ASUS		Title : EMI&Shield case	
ASUS&K COMPUTER		Engineer: EE	
Size B	Project Name	GX550LXS	
Date: Wednesday, February 19, 2020	Sheet	59 of 103	Rev R1.0

DC-IN Connector

DC Jack使用請詢用River_Hsu

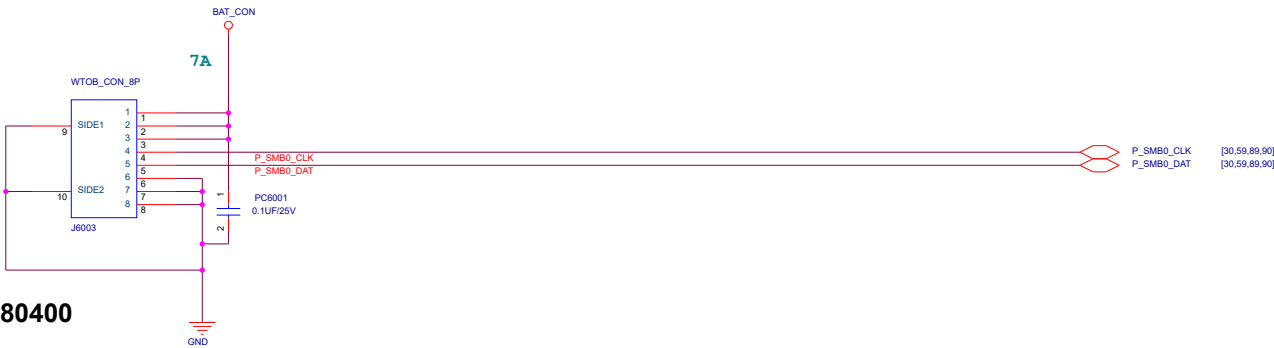
New 6 Phi 4 Pin DC_Jack 1.55ch



12033-00020300


J6001	3.4CH	1.55CH
	12033-00020200	12033-00020300

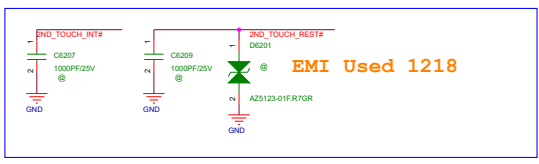
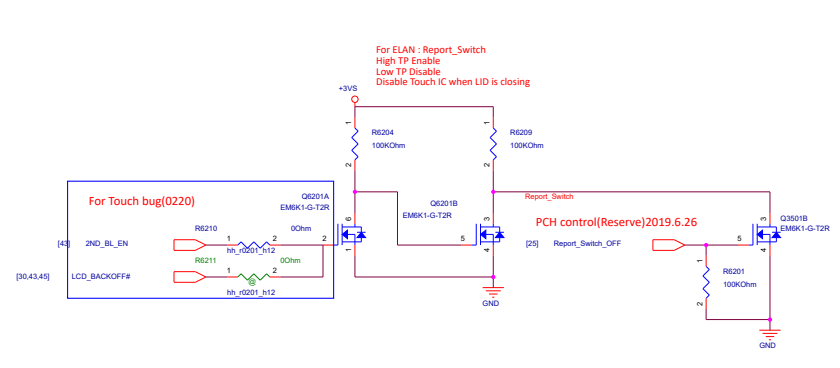
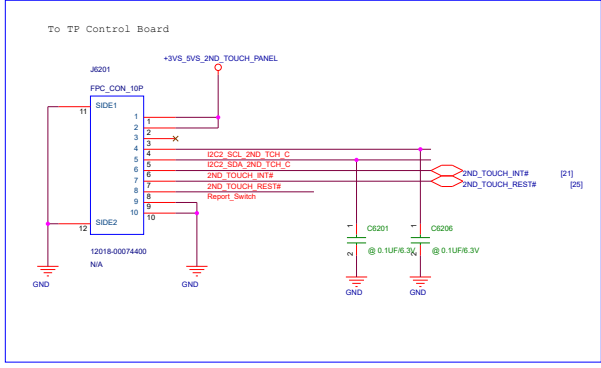
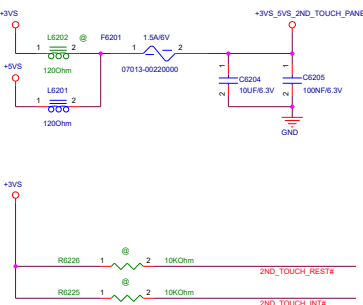
Battery Connector



12017-00080400

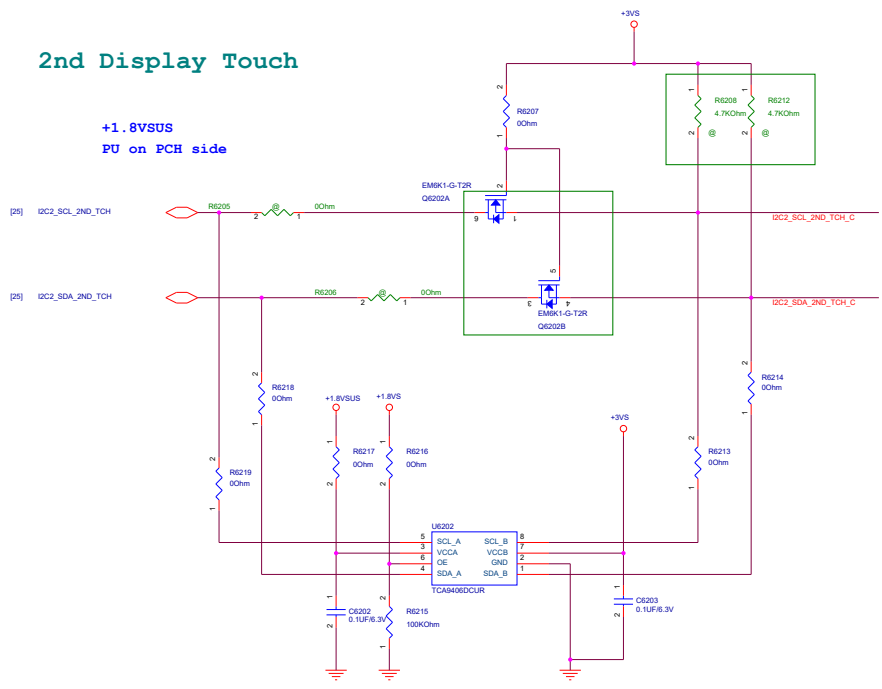
Note: Battery Connector 正確性與BAT1_IN_OC#是否預留!

		Title : BT_Blueetooth	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX550LXS		Rev R1.0
Date: Wednesday, February 19, 2020		Sheet 61 of 103	



2nd Display Touch

+1.8VSUS
PU on PCH side





Project Name

GX550LXS

Rev

R1.0

Title : **TOUCH_2**

Size

B

Dept.: **NB_Power team**

Engineer: **Benson**

Date: **Wednesday, February 19, 2020**

Sheet **63** of **103**



Project Name

GX550LXS

Rev

R1.0

Title : **TBT_TBT IC_DP_R2.0a**

Size

C

Dept.: **ASUSTeK COMPUTER INC. NB1**

Engineer: **EE1_RD3**

Date: **Wednesday, February 19, 2020**

Sheet **64** of **103**



Project Name

GX550LXS

Rev

R1.0

Title : **B key**

Size

C

Dept.:

ASUSTeK COMPUTER INC. NB1

Engineer:

EE1_RD3

Date: **Wednesday, February 19, 2020**

Sheet

66

of

103



Project Name

GX550LXS

Rev

R1.0

Title : **TBT_TBT IC_DP_R2.0a**


Size


B

Dept.: **ASUSTeK COMPUTER INC. NB1** **Engineer:** **EE1_RD3**

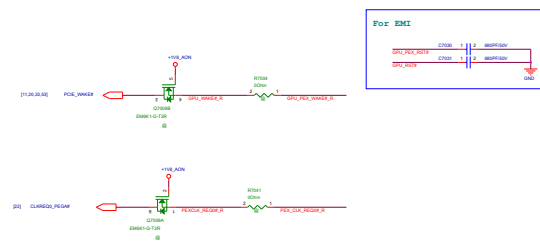
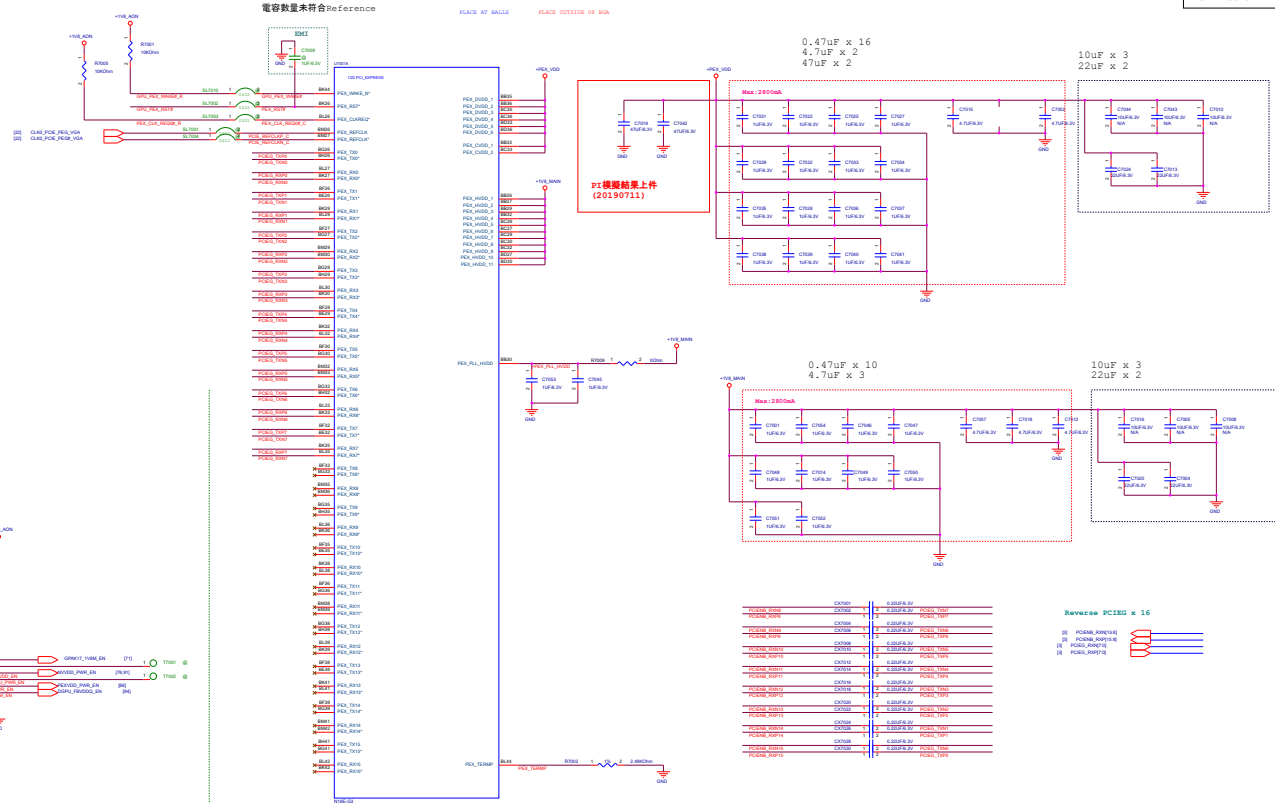
Date: **Wednesday, February 19, 2020**

Sheet **67** of **103**

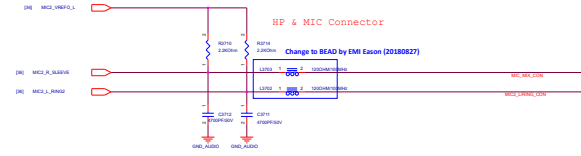
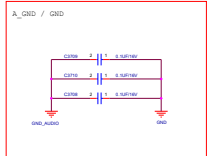
		Title : OTH_for test only	
ASUSTeK COMPUTER		Engineer: EE	
Size	Project Name		Rev
C	teknisi-indonesia GX550LXS		R1.0
Date: Wednesday, February 19, 2020		Sheet 68 of 103	

		Title : <Title>	
ASUSTeK COMPUTER		Engineer: EE	
Size B	Project Name GX550LXS		Rev R1.0
Date: Wednesday, February 19, 2020		Sheet 69 of 103	

GPU分2080/2070，共用線路，用BOM區分
GPU料號如下
2080：02004-00573600
2070：02004-00573500



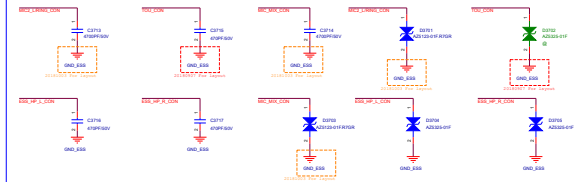
Headphone&MIC



HP & MIC Connector

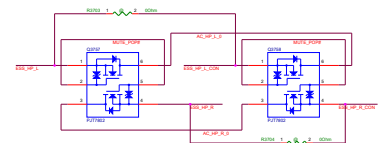


EMI



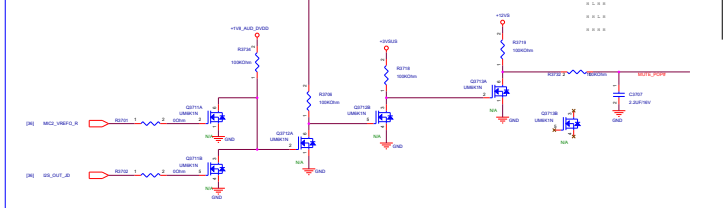
MUTE

2019.02.24 Modify MUTE action (New low side on)

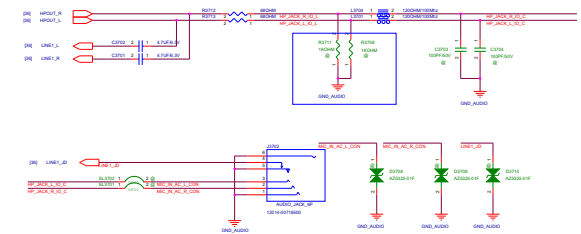


MUTE Control

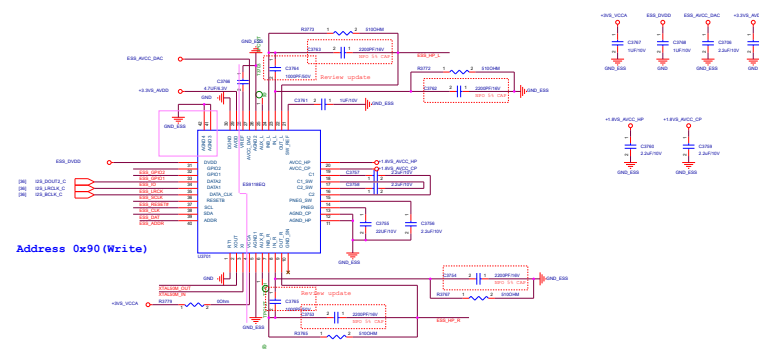
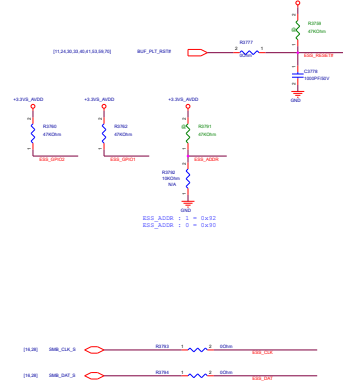
2016.07.22 New MUTE action



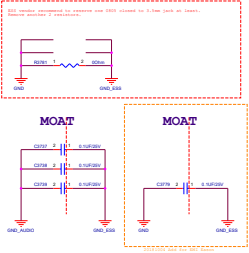
EXTERNAL MICROPHONE



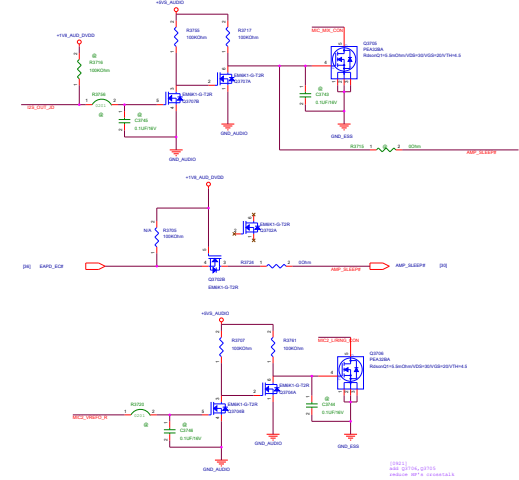
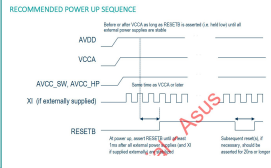
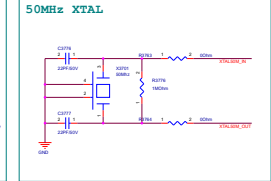
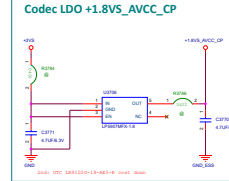
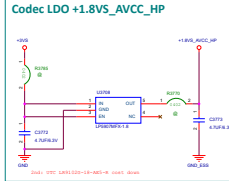
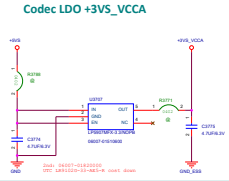
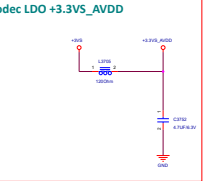
ESS ES9118EQ



Address 0x90 (Write)



Modify 1216



Driver 行為會follow 下表

	ES9118EQ	ES9118EQ	ES9118EQ
ES9118EQ	ES9118EQ	ES9118EQ	ES9118EQ
ES9118EQ	ES9118EQ	ES9118EQ	ES9118EQ
ES9118EQ	ES9118EQ	ES9118EQ	ES9118EQ
ES9118EQ	ES9118EQ	ES9118EQ	ES9118EQ
ES9118EQ	ES9118EQ	ES9118EQ	ES9118EQ
ES9118EQ	ES9118EQ	ES9118EQ	ES9118EQ
ES9118EQ	ES9118EQ	ES9118EQ	ES9118EQ
ES9118EQ	ES9118EQ	ES9118EQ	ES9118EQ
ES9118EQ	ES9118EQ	ES9118EQ	ES9118EQ

40 Ohm NET
FBA Partition 31..0
MF=1 Mirror

[72] FBA_DB1..0

FBA_CMD[33..0]

[72] FBA_DB1..0

FBA_CMD[33..0]

待機Samsung
03014-00010100

U73001

FBA_D4 B4 DQ0_A
FBA_D7 B3 DQ1_A
FBA_D1 B2 DQ2_A
FBA_D3 B1 DQ3_A
FBA_D5 E3 DQ4_A
FBA_D3 B1 DQ3_A
FBA_D6 F2 DQ5_A
FBA_D3 B1 DQ3_A
FBA_D2 G2 DQ7_A
FBA_D6 B1 DQ8_A
FBA_D15 A12 DQ9_A
FBA_D13 B12 DQ10_A
FBA_D14 E12 DQ11_A
FBA_D12 E13 DQ12_A
FBA_D11 E13 DQ13_A
FBA_D11 E13 DQ14_A
FBA_D11 E13 DQ15_A

FBA_CMD0 H3 CA0_A
FBA_CMD9 G11 CA1_A
FBA_CMD9 H2 CA2_A
FBA_CMD8 H2 CA3_A
FBA_CMD32 H6 CA4_A
FBA_CMD7 H10 CA5_A
FBA_CMD11 H2 CA6_A
FBA_CMD15 J11 CA7_A
FBA_CMD14 J4 CA8_A
FBA_CMD3 J3 CA9_A
FBA_CMD1 J5 CAB1_n_A
FBA_CMD6 G10 CKE_n_A

[72] FBA_DB0 FBA_DB1 D2 DBI0_n_A
[72] FBA_DB1 D13 DBI1_n_A
[72] FBA_WCK0 FBA_WCK1# D4 WCK1_n_A
[72] FBA_WCK1# D5 WCK_c_A

[72] FBA_EDC0 FBA_EDC1 C2 EDC0_A
[72] FBA_EDC1 C13 EDC1_A

FBA_D30 V3 DQ0_B
FBA_D19 U3 DQ1_B
FBA_D28 U2 DQ2_B
FBA_D31 P3 DQ3_B
FBA_D19 U3 DQ4_B
FBA_D27 N2 DQ5_B
FBA_D24 M2 DQ7_B
FBA_D19 U3 DQ8_B
FBA_D23 V12 DQ9_B
FBA_D22 U7 DQ10_B
FBA_D20 U3 DQ11_B
FBA_D17 P12 DQ12_B
FBA_D21 P13 DQ13_B
FBA_D18 M13 DQ14_B
FBA_D18 M13 DQ15_B

FBA_CMD4 L3 CA0_B
FBA_CMD12 M1 CA1_B
FBA_CMD12 M4 CA2_B
FBA_CMD5 L12 CA3_B
FBA_CMD13 L8 CA4_B
FBA_CMD7 K12 CA5_B
FBA_CMD14 K11 CA6_B
FBA_CMD15 K4 CA7_B
FBA_CMD3 K3 CA8_B
FBA_CMD1 K5 CA9_B
FBA_CMD6 M10 CAB1_n_B
FBA_CMD10 M10 CKE_n_B

[72] FBA_DB3 FBA_DB2 R2 DBI0_n_B
[72] FBA_DB2 R13 DBI1_n_B

[72] FBA_WCK23 FBA_WCK23# R11 WCK1_n_B
[72] FBA_WCK23# R10 WCK_c_B

[72] FBA_EDC3 FBA_EDC2 T2 EDC0_B
[72] FBA_EDC2 T13 EDC1_B

[72] FBA_CLK0# FBA_CLK0 K10 CK_c
[72] FBA_CLK0 K10 CK_1

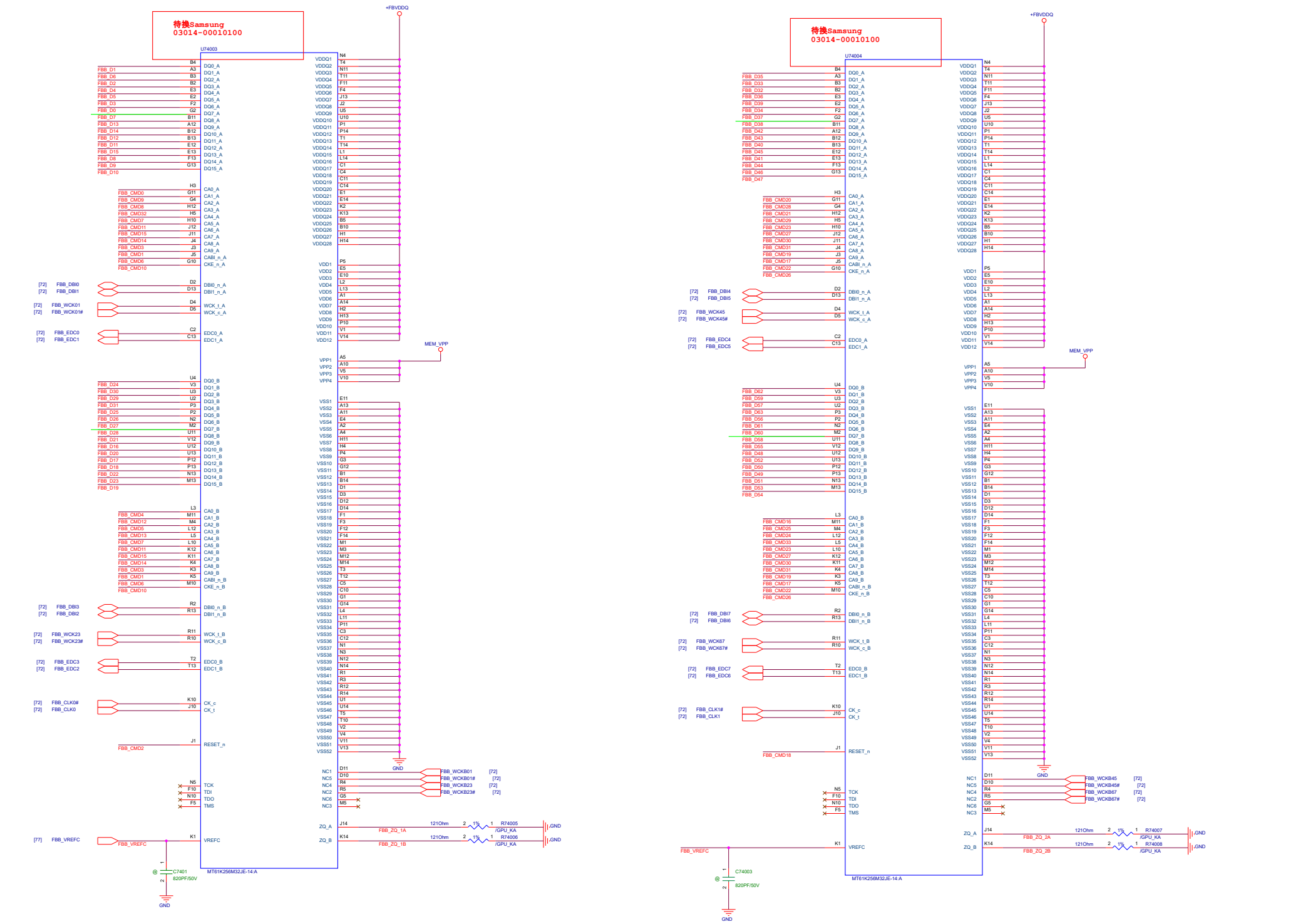
FBA_CMD2 J1 RESET_n

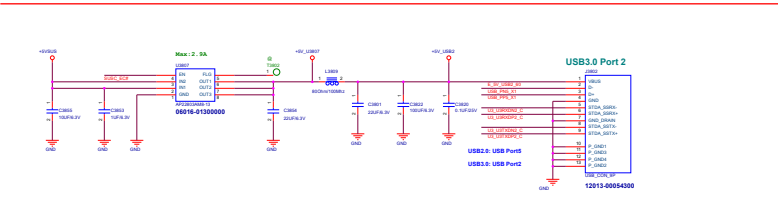
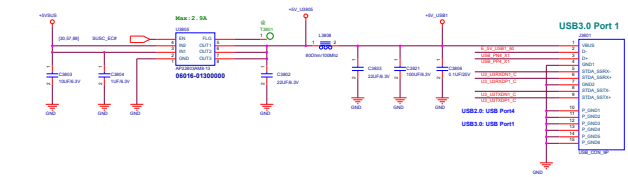
[72] FBA_VREFC FBA_VREFC K1 VREFC



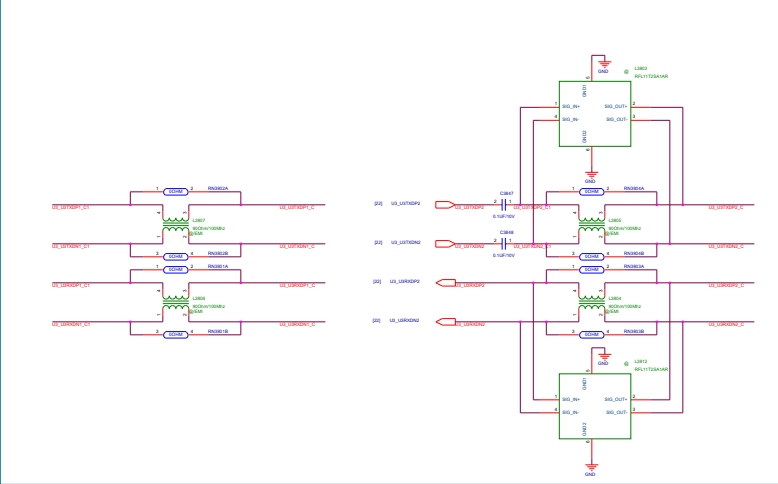
MT61K25M32JE-14A

+FBVDDQ
VDD01 T4
VDD02 N11
VDD03 T11
VDD04 F11
VDD05 F4
VDD06 F2
VDD07 Z2
VDD08 U10
VDD09 B11
VDD10 P1
VDD11 P14
VDD12 T1
VDD13 T14
VDD14 L1
VDD15 L14
VDD16 C1
VDD17 C4
VDD18 C14
VDD19 E1
VDD20 E14
VDD21 K2
VDD22 K13
VDD23 B5
VDD24 B10
VDD25 H1
VDD26 H4
VDD27 P5
VDD28 E5
VDD29 E10
VDD30 L2
VDD31 L13
VDD32 A1
VDD33 A14
VDD34 H2
VDD35 H13
VDD36 P10
VDD37 V1
VDD38 V14
VDD39 A5
VDD40 A10
VDD41 V10
VDD42 E11
VDD43 A13
VDD44 E4
VDD45 A2
VDD46 J4
VDD47 H1
VDD48 H4
VDD49 P4
VDD50 G3
VDD51 G12
VDD52 B1
VDD53 B14
VDD54 D1
VDD55 D3
VDD56 D12
VDD57 D14
VDD58 F1
VDD59 F3
VDD60 F12
VDD61 F14
VDD62 M1
VDD63 M3
VDD64 M12
VDD65 M14
VDD66 T3
VDD67 T12
VDD68 C5
VDD69 C16
VDD70 G14
VDD71 L4
VDD72 L11
VDD73 T1
VDD74 C3
VDD75 C12
VDD76 NT
VDD77 N3
VDD78 N12
VDD79 N14
VDD80 R1
VDD81 R3
VDD82 R12
VDD83 R14
VDD84 U1
VDD85 U14
VDD86 T5
VDD87 T10
VDD88 V4
VDD89 V11
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VDD





USB3.0 EMI-Protection



R1.6 USB2.0 EMI-Protection With ECMF (PCB 1.05mm_12Layer)

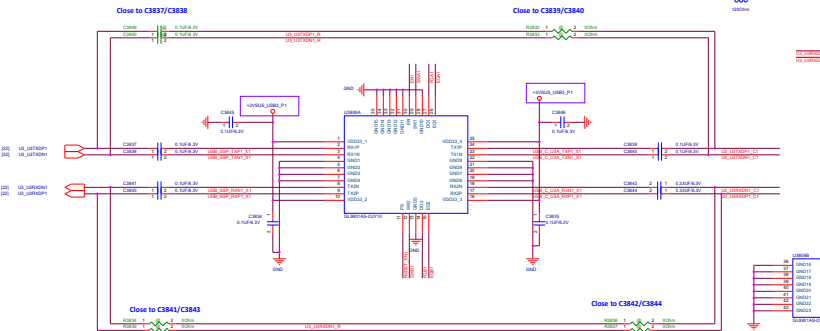


1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
2. C3813&C3819 must be replaced with 20pF C201 capacitors and the tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
4. Pin13 to Pin16 are floated in regular scheme

temp_M08_000007層名順序是：TOP/GND/IN1/GND1/IN2/VCC/VCC1/IN3/GND2/IN4/GND3/BOTTOM

USB3.1_Port1 (Gen2)

[Bypass Path]



< Fine tune table for Pericom (One port Gen2) >

ESDA[R]	Gen 1 (S550)[R]	Gen 2 (S550)[R]
0: 0 Ω to GND	5.1	10.0
R: Resist to GND	1.9	6.7
F: Leave Open	3.5(Default)	6.1(Default)
1: 0 Ω to VDD	6.8	13.1

Note: With internal 100kOhm pull-up Rpg and 200kOhm pull-down Rdown.

Ref: = S5500m

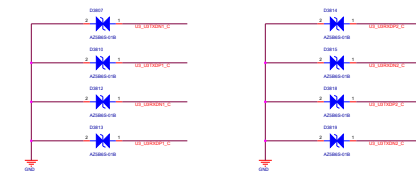
< FG table for Pericom 1002B >

ESDA[R]	Flar Gain [dB]
0: 0 Ω to GND	-0.0
R: Resist to GND	-1.5
F: Leave Open	0 (Default)
1: 0 Ω to VDD	+2.0

< SW table for Pericom 1002B >

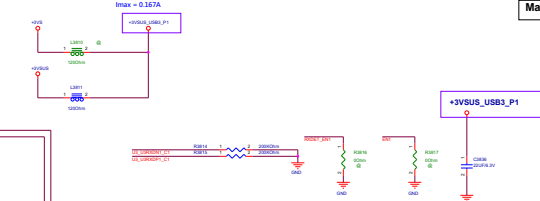
ESDA[R]	Output Linear Setting [mV]
0: 0 Ω to GND	800
R: Resist to GND	1200
F: Leave Open	1000 (Default)
1: 0 Ω to VDD	1200

USB3.0 ESD-Protection



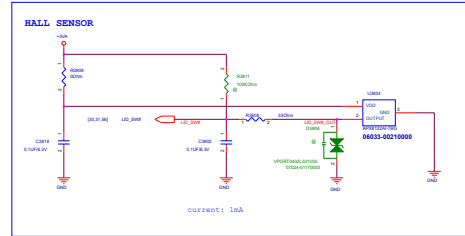
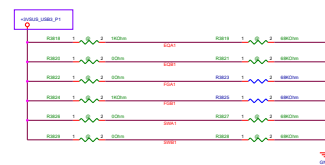
ESD PROTECTION
Part Number: P10-07024-013600000 ESD PROTECTION A2060-01B

ESD PROTECTION
Part Number: P10-07024-013600000 ESD PROTECTION A2060-01B

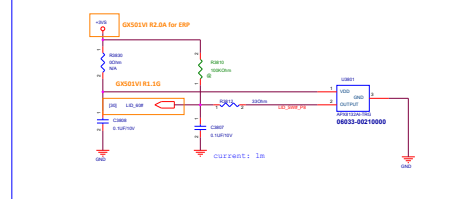


< Channel / Receiver setting for Pericom 1002B >

Setting	Channel Enable [N]	Receiver Detection [REDET_N]
0: 0 Ω to GND	Disable	Disable
1: 0 Ω to VDD	Enable(Default)	Enable(Default)
New	Channel Enable / Receiver detection With internal 200K pull-up R.	



HALL SENSOR for 60 degree

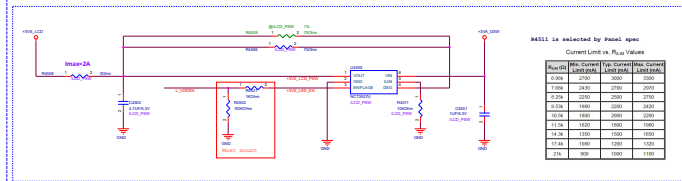
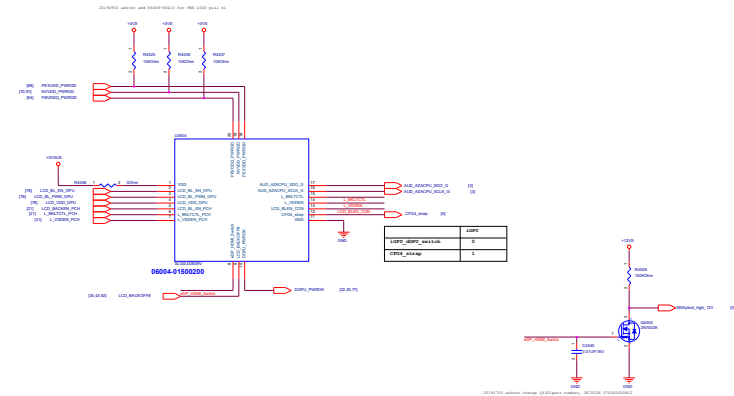


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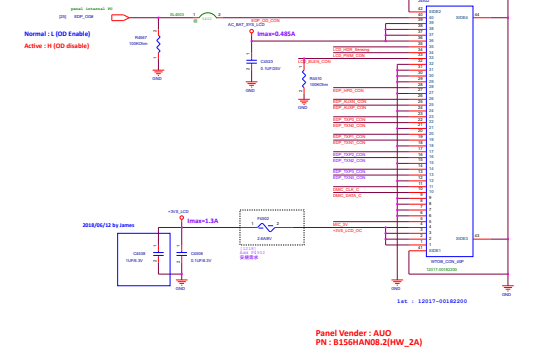
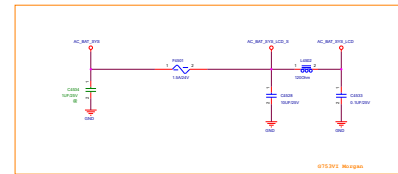
BL_EN/BL_PWM/L_VDDEN SWITCH IC(Switchable Use)

LCD Power switch

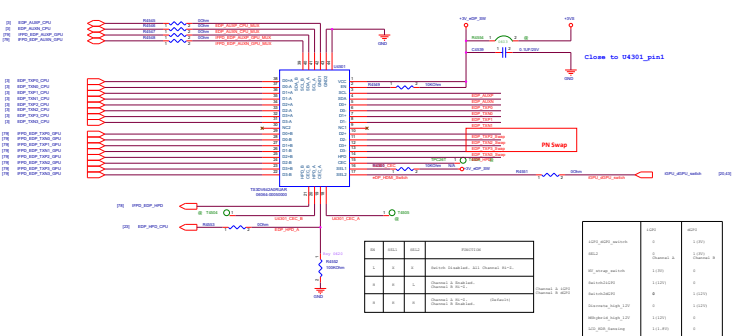
eDP Panel Conn.



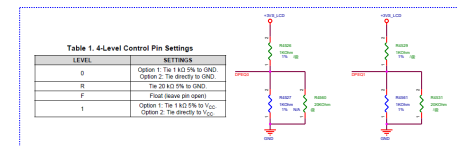
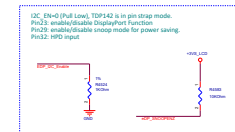
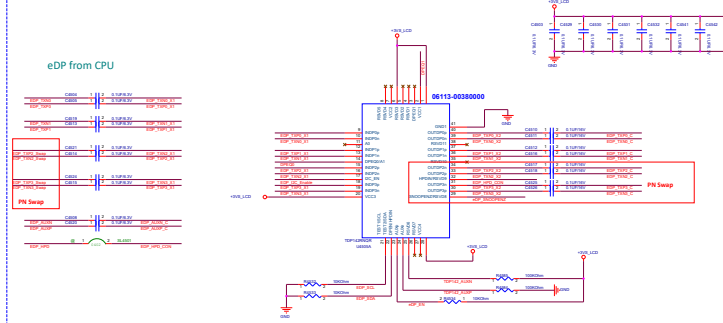
Panel BL Power



eDP Switch



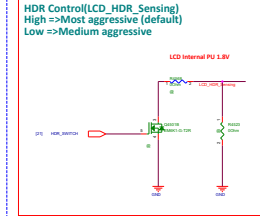
EDP1.4 Re-driver



For EMI

For ESD

20181204(HDR Panel Pin34 Use)



eDP_HP(D CPU)

Cable Detect

eDP_BL PWM

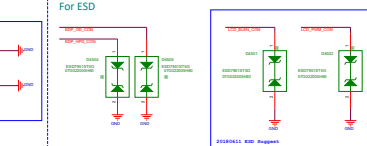
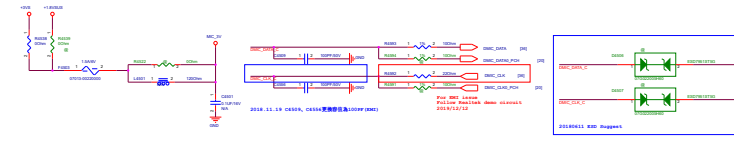


Pin No.	Symbol	Pin No.	Symbol
1	NC	34	CD-GND
2	H-GND	35	CD-GND
3	lane3_P	36	CD-GND
4	lane3_P	37	HPD
5	H-GND	38	BL-GND
6	lane2_P	39	BL-GND
7	lane2_P	40	BL-GND
8	H-GND	41	BL-GND
9	lane1_P	42	BL-Enable
10	lane1_P	43	BL-PWM DTM
11	H-GND	44	NC
12	lane0_P	45	NC
13	lane0_P	46	BL-PWR
14	H-GND	47	BL-PWR
15	AUX_CH_P	48	BL-PWR
16	AUX_CH_N	49	BL-PWR
17	H-GND	50	NC
18	CD-VCC		
19	CD-VCC		
20	CD-VCC		
21	CD-VCC		
22	CD-Self_Test		
23	CD-GND		

MIC module

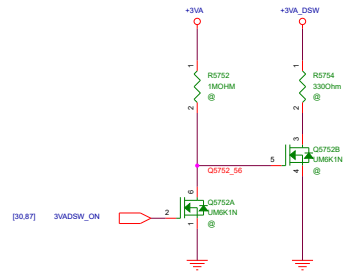
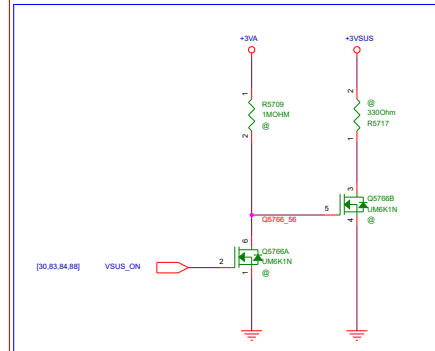
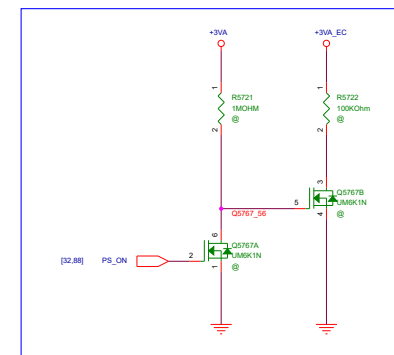
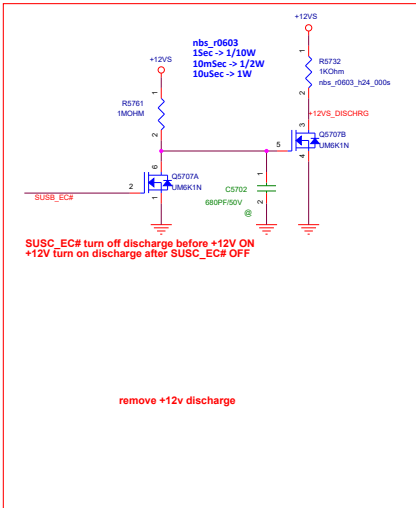
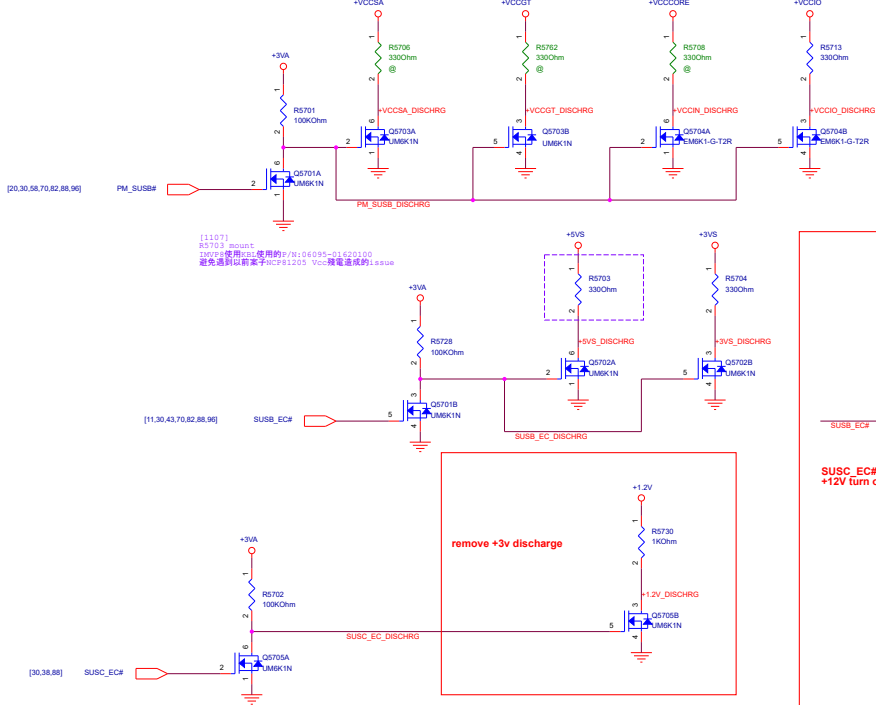
MIC

For ESD

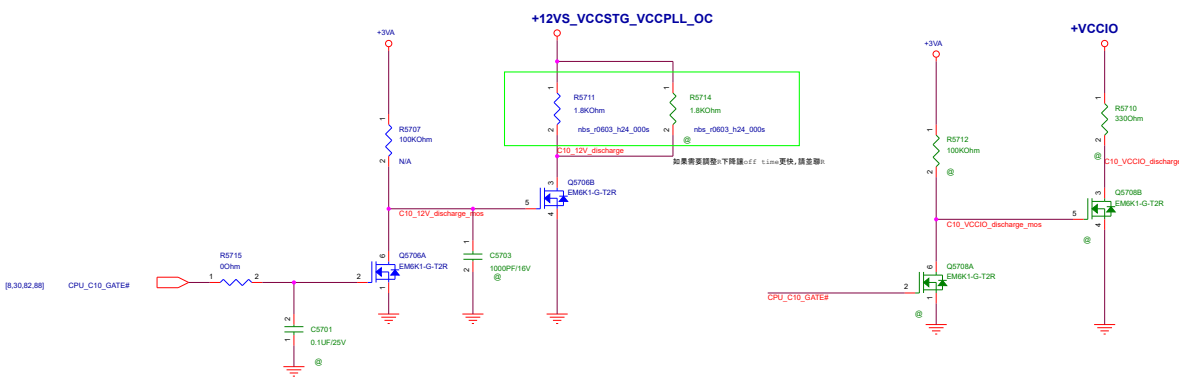


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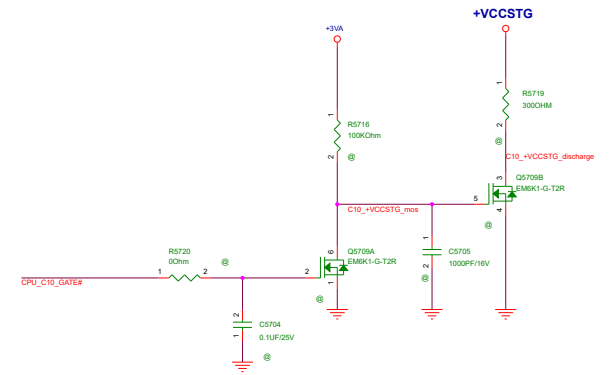
For ESD



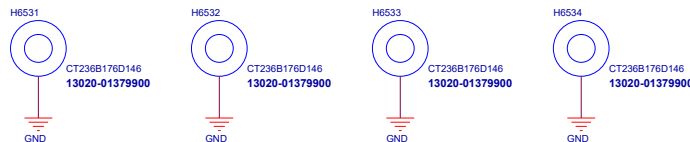
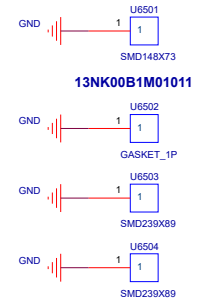
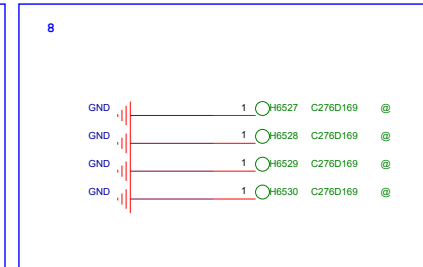
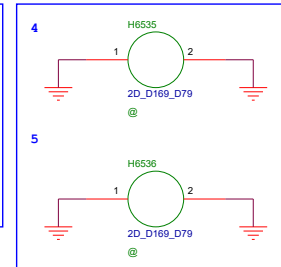
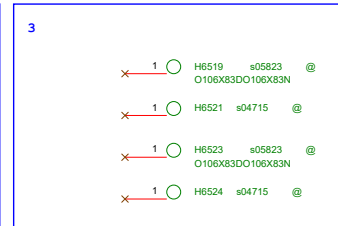
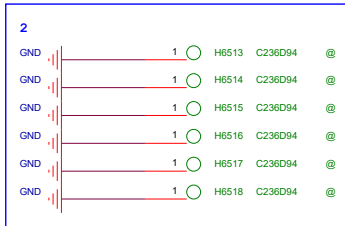
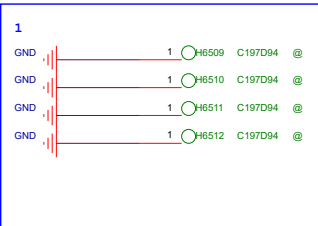
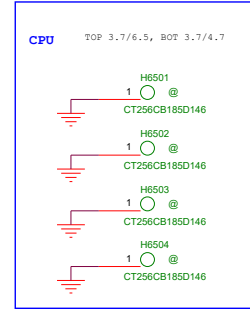
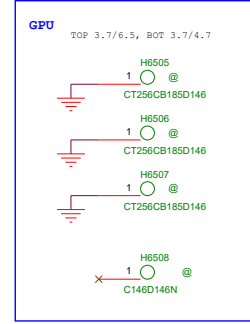
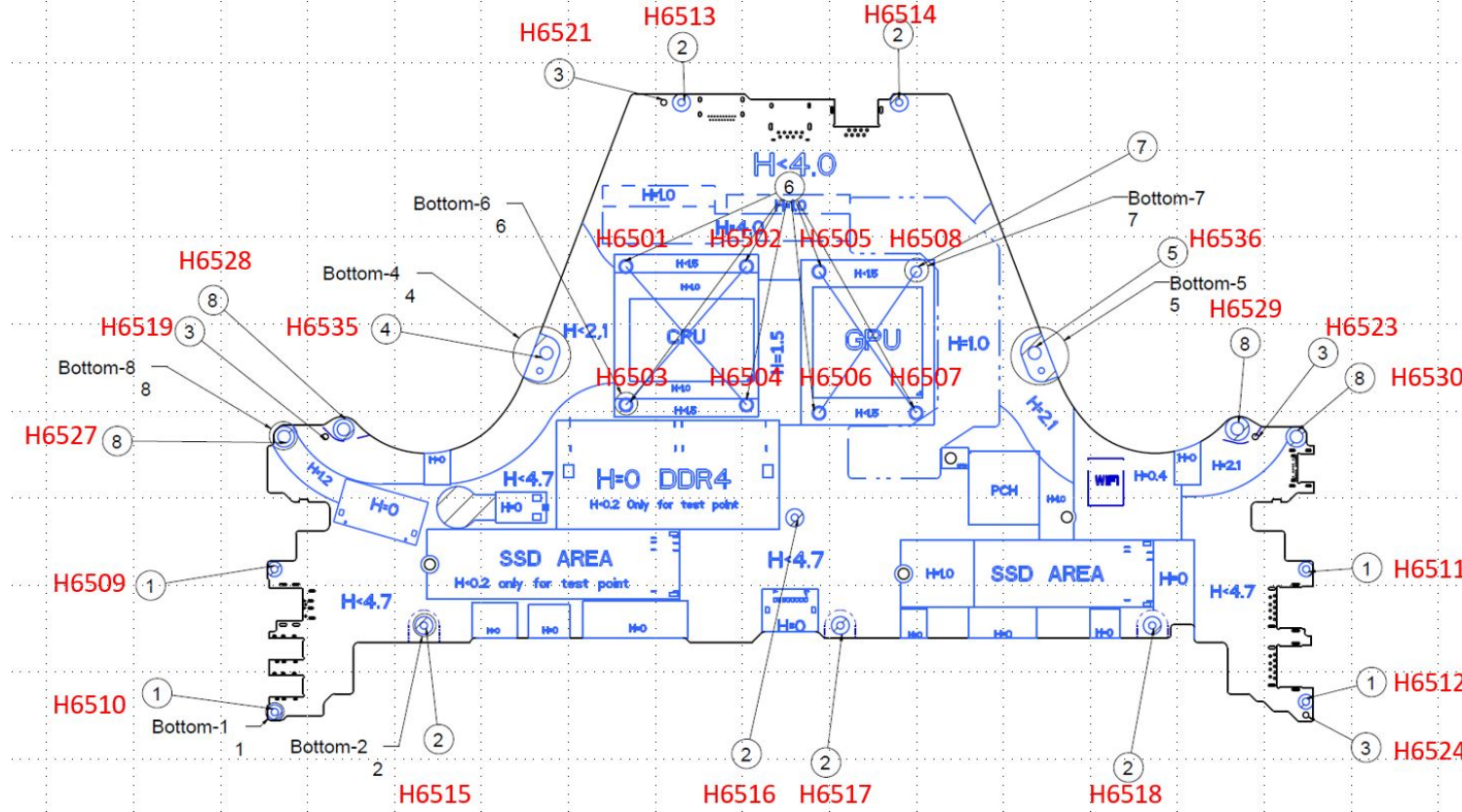
20191106 增加discharge schematic for C10, VCCIO unmount for reserve



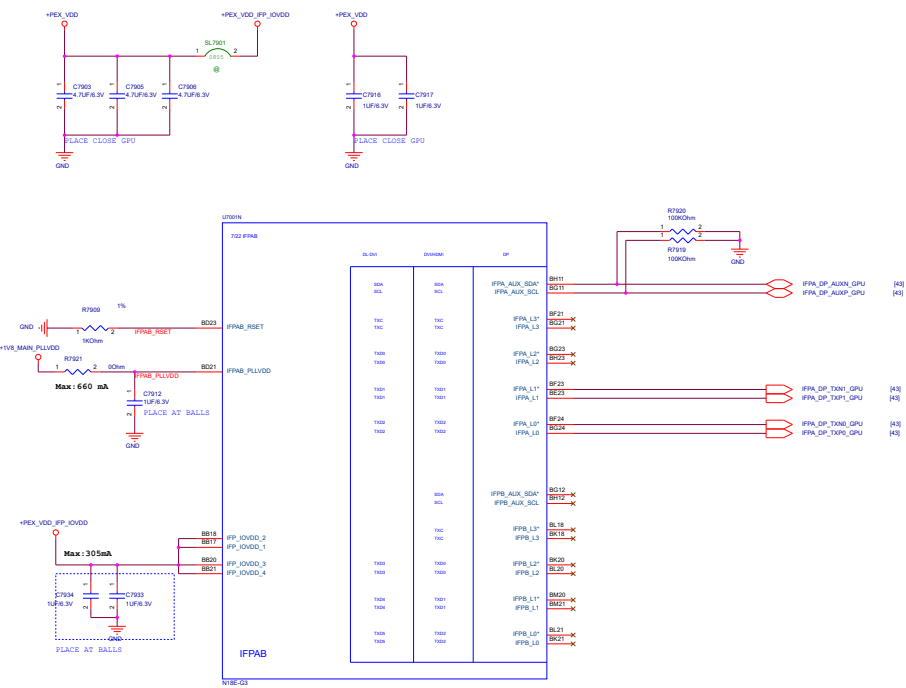
20191218 預置+VCCSTGdischarge schematic for C10



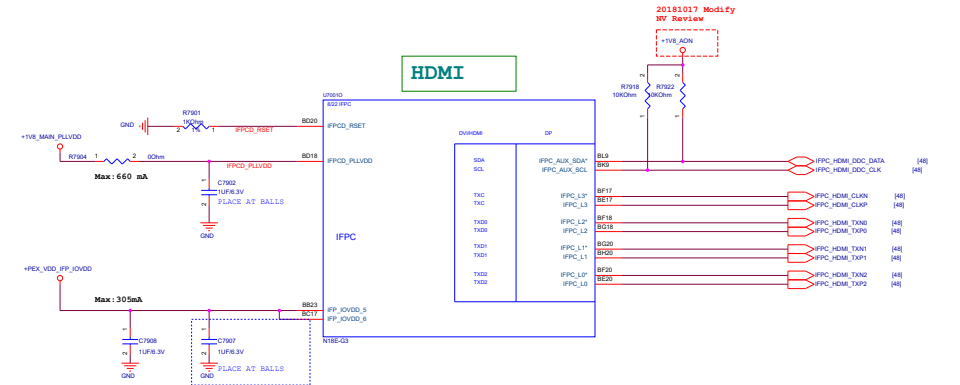
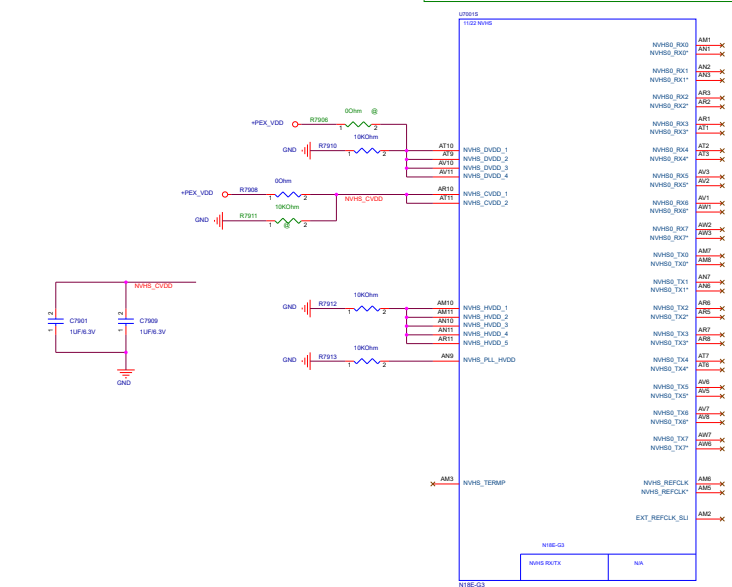
+Core Design



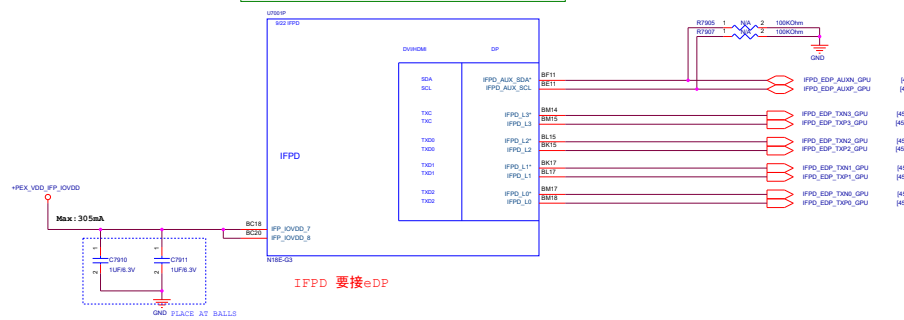
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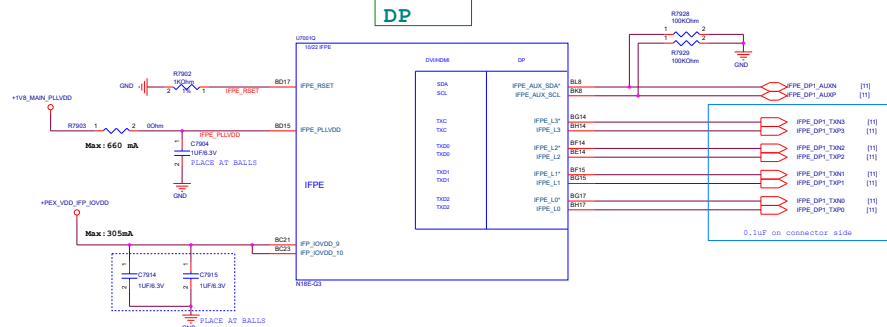
NVLink (not used)



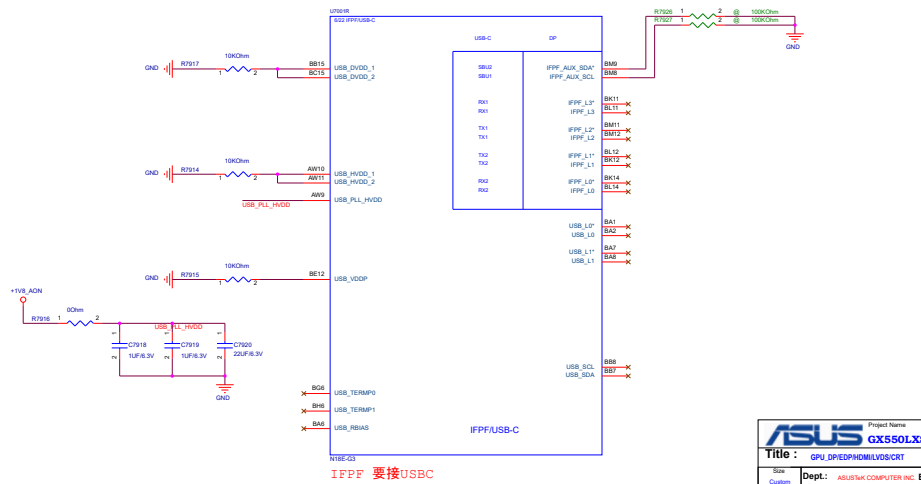
EDP (4Lane Panel)



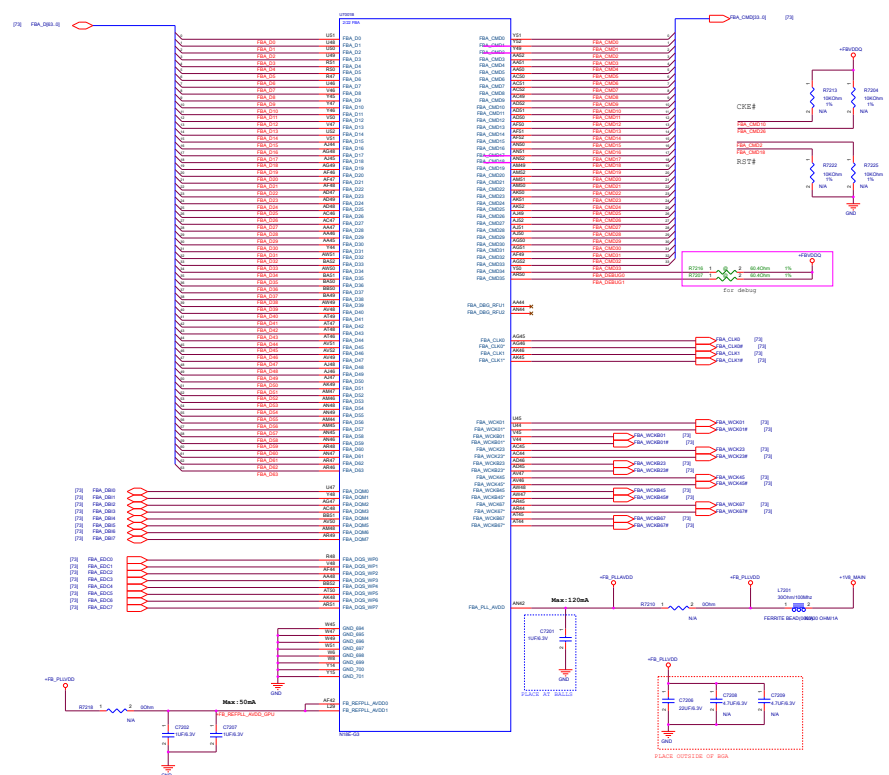
DP



USB-C/DP (not used)

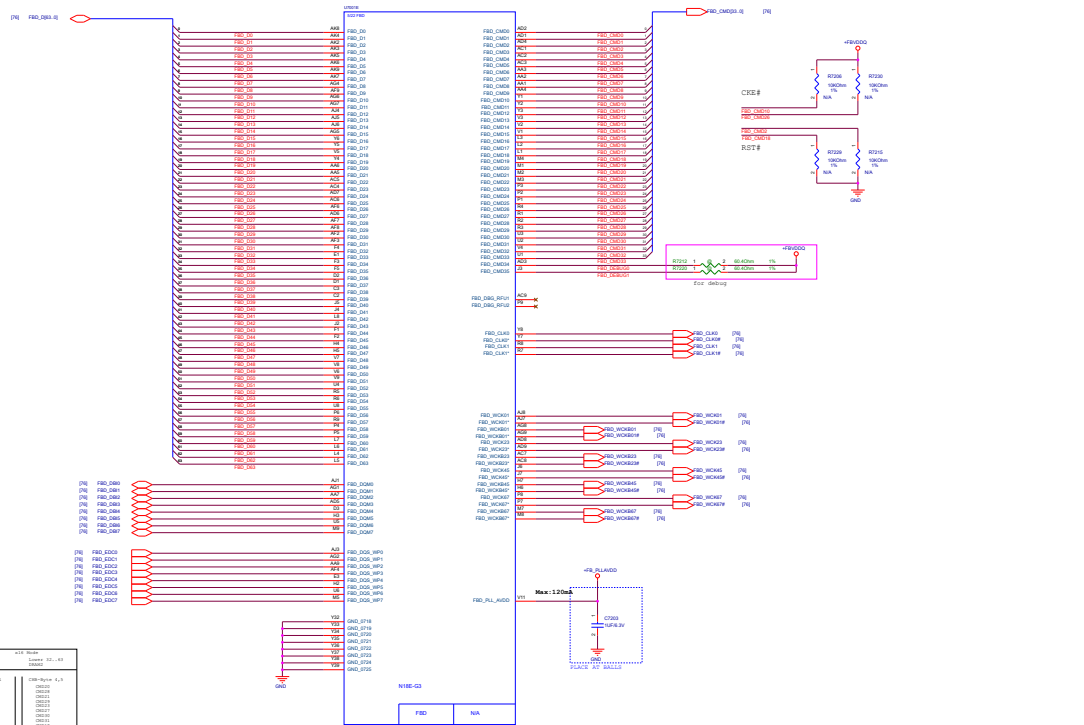


MEMORY: GPU FB Partition A

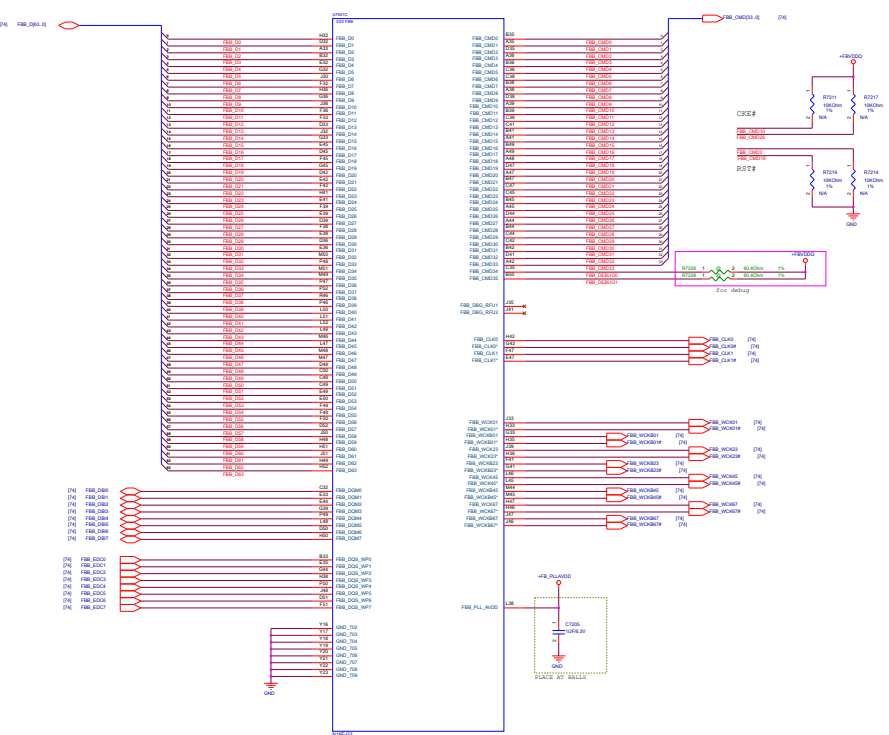


SS204	CRS	Response	axis	Range
		Location 1, -33		Location 22, -63
		CRMS		CRMS2
		CRS-Rtype 1,1		CRS-Rtype 4,9
CRS_1		CRMS1		CRMS10
CRS_2		CRMS2		CRMS11
CRS_3		CRMS3		CRMS12
CRS_4		CRMS4		CRMS13
CRS_5		CRMS5		CRMS14
CRS_6		CRMS6		CRMS15
CRS_7		CRMS7		CRMS16
CRS_8		CRMS8		CRMS17
CRS_9		CRMS9		CRMS18
CRS_10		CRMS10		CRMS19
CRS_11		CRMS11		CRMS20
CRS_12		CRMS12		CRMS21
CRS_13		CRMS13		CRMS22
CRS_14		CRMS14		CRMS23
CRS_15		CRMS15		CRMS24
CRS_16		CRMS16		CRMS25
CRS_17		CRMS17		CRMS26
CRS_18		CRMS18		CRMS27
CRS_19		CRMS19		CRMS28
CRS_20		CRMS20		CRMS29
CRS_21		CRMS21		CRMS30
CRS_22		CRMS22		CRMS31
CRS_23		CRMS23		CRMS32
CRS_24		CRMS24		CRMS33
CRS_25		CRMS25		CRMS34
CRS_26		CRMS26		CRMS35
CRS_27		CRMS27		CRMS36
CRS_28		CRMS28		CRMS37
CRS_29		CRMS29		CRMS38
CRS_30		CRMS30		CRMS39
CRS_31		CRMS31		CRMS40
CRS_32		CRMS32		CRMS41
CRS_33		CRMS33		CRMS42
CRS_34		CRMS34		CRMS43
CRS_35		CRMS35		CRMS44
CRS_36		CRMS36		CRMS45
CRS_37		CRMS37		CRMS46
CRS_38		CRMS38		CRMS47
CRS_39		CRMS39		CRMS48
CRS_40		CRMS40		CRMS49
CRS_41		CRMS41		CRMS50
CRS_42		CRMS42		CRMS51
CRS_43		CRMS43		CRMS52
CRS_44		CRMS44		CRMS53
CRS_45		CRMS45		CRMS54
CRS_46		CRMS46		CRMS55
CRS_47		CRMS47		CRMS56
CRS_48		CRMS48		CRMS57
CRS_49		CRMS49		CRMS58
CRS_50		CRMS50		CRMS59
CRS_51		CRMS51		CRMS60
CRS_52		CRMS52		CRMS61
CRS_53		CRMS53		CRMS62
CRS_54		CRMS54		CRMS63
CRS_55		CRMS55		CRMS64
CRS_56		CRMS56		CRMS65
CRS_57		CRMS57		CRMS66
CRS_58		CRMS58		CRMS67
CRS_59		CRMS59		CRMS68
CRS_60		CRMS60		CRMS69
CRS_61		CRMS61		CRMS70
CRS_62		CRMS62		CRMS71
CRS_63		CRMS63		CRMS72
CRS_64		CRMS64		CRMS73
CRS_65		CRMS65		CRMS74
CRS_66		CRMS66		CRMS75
CRS_67		CRMS67		CRMS76
CRS_68		CRMS68		CRMS77
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CRS_70		CRMS70		CRMS79
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CRS_73		CRMS73		CRMS82
CRS_74		CRMS74		CRMS83
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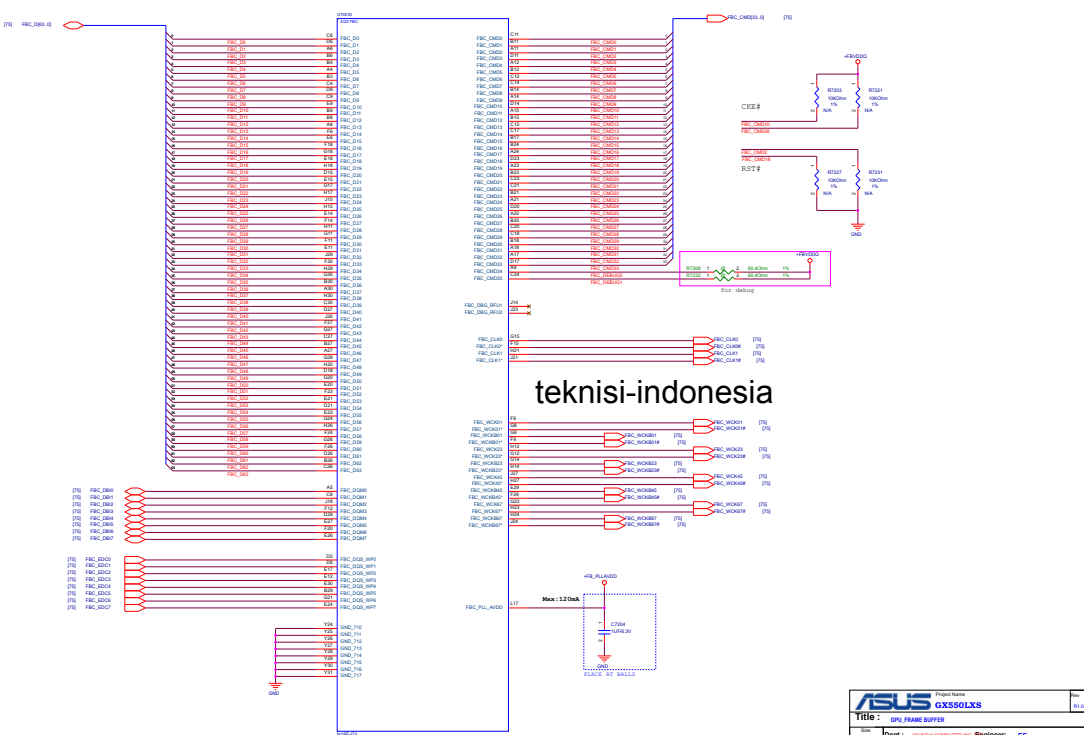
MEMORY: GPU FB Partition D

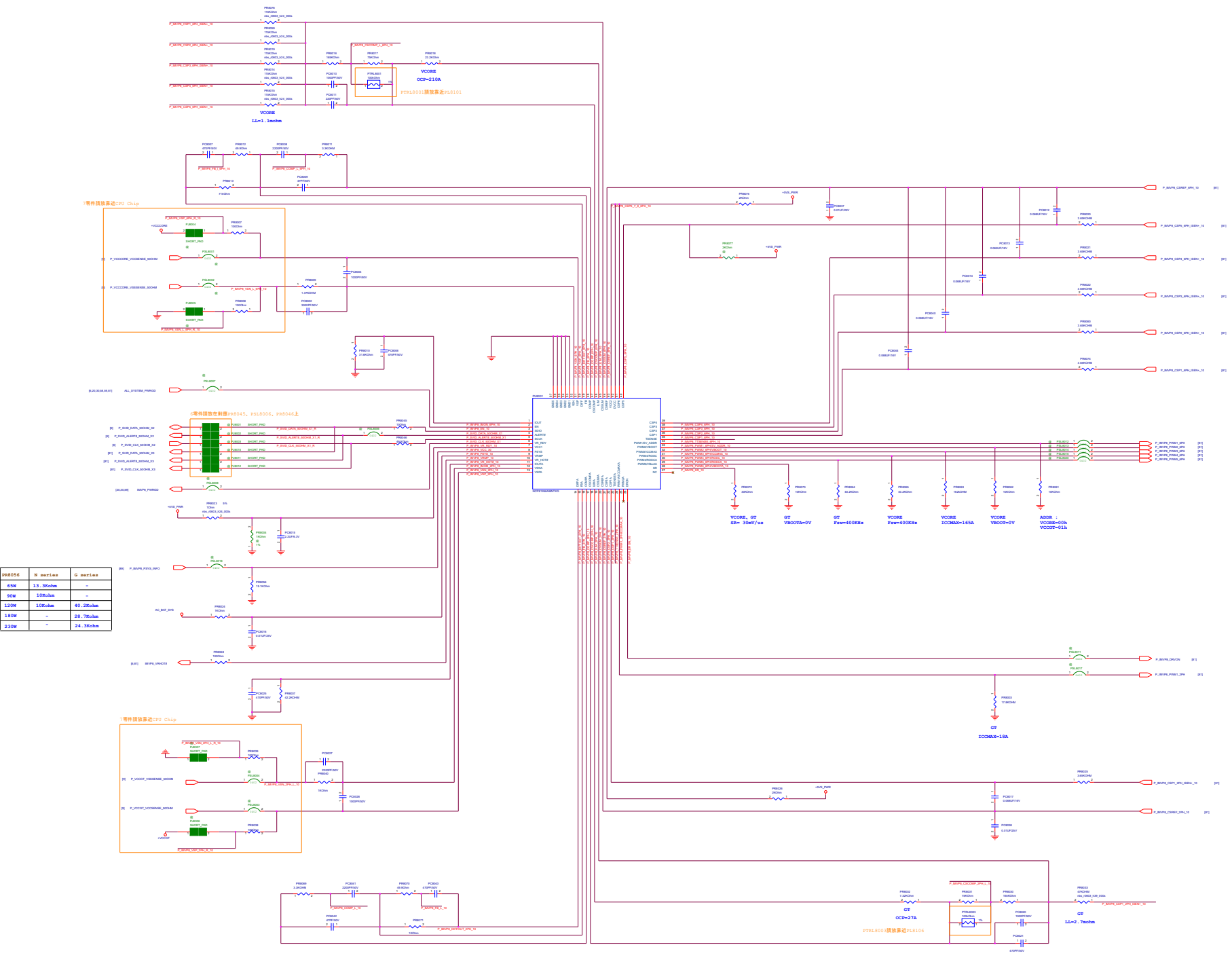


MEMORY: GPU FB Partition B

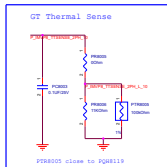
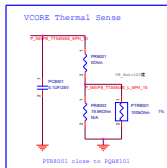


MEMORY: GPU FB Partition C

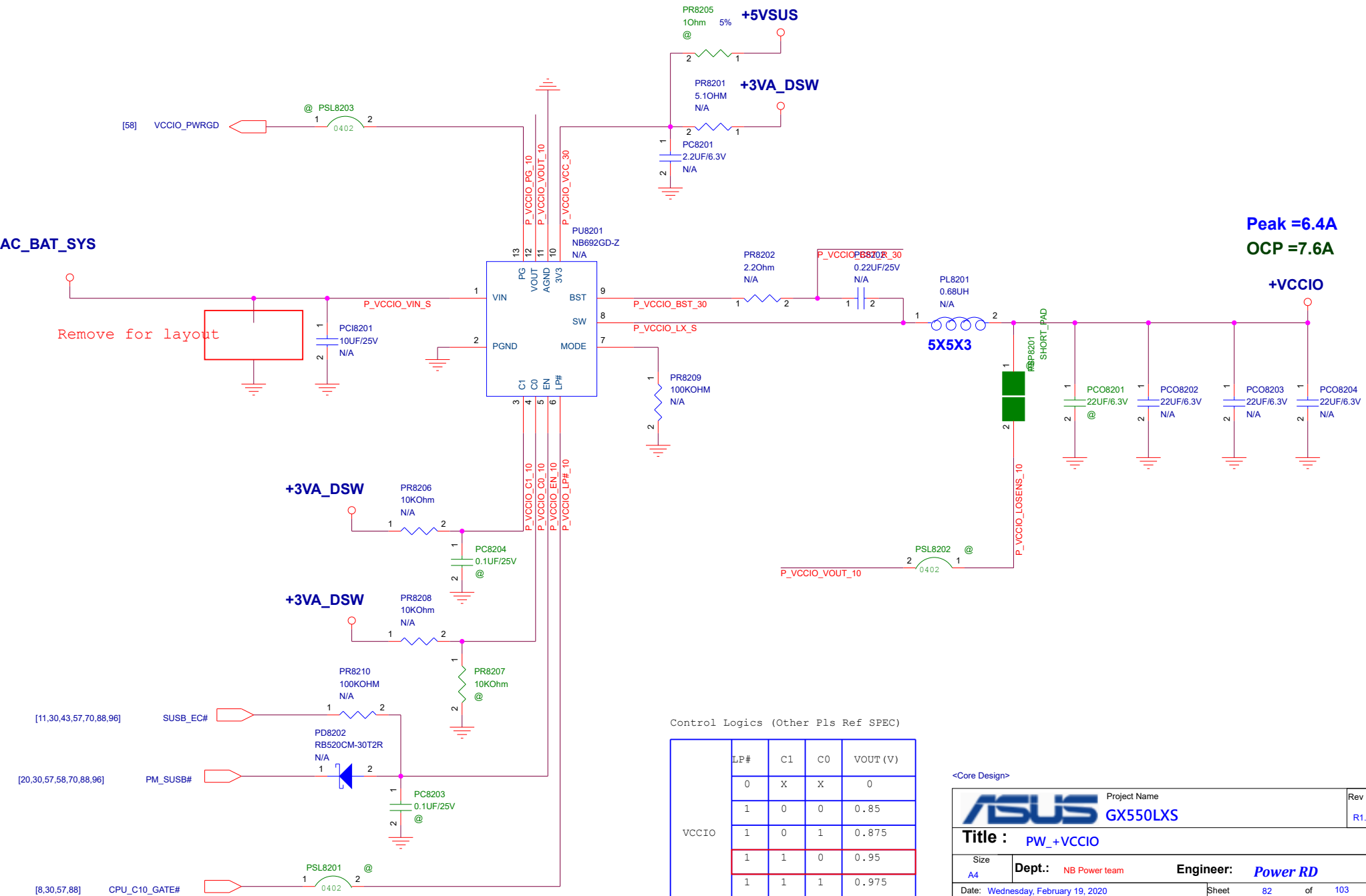




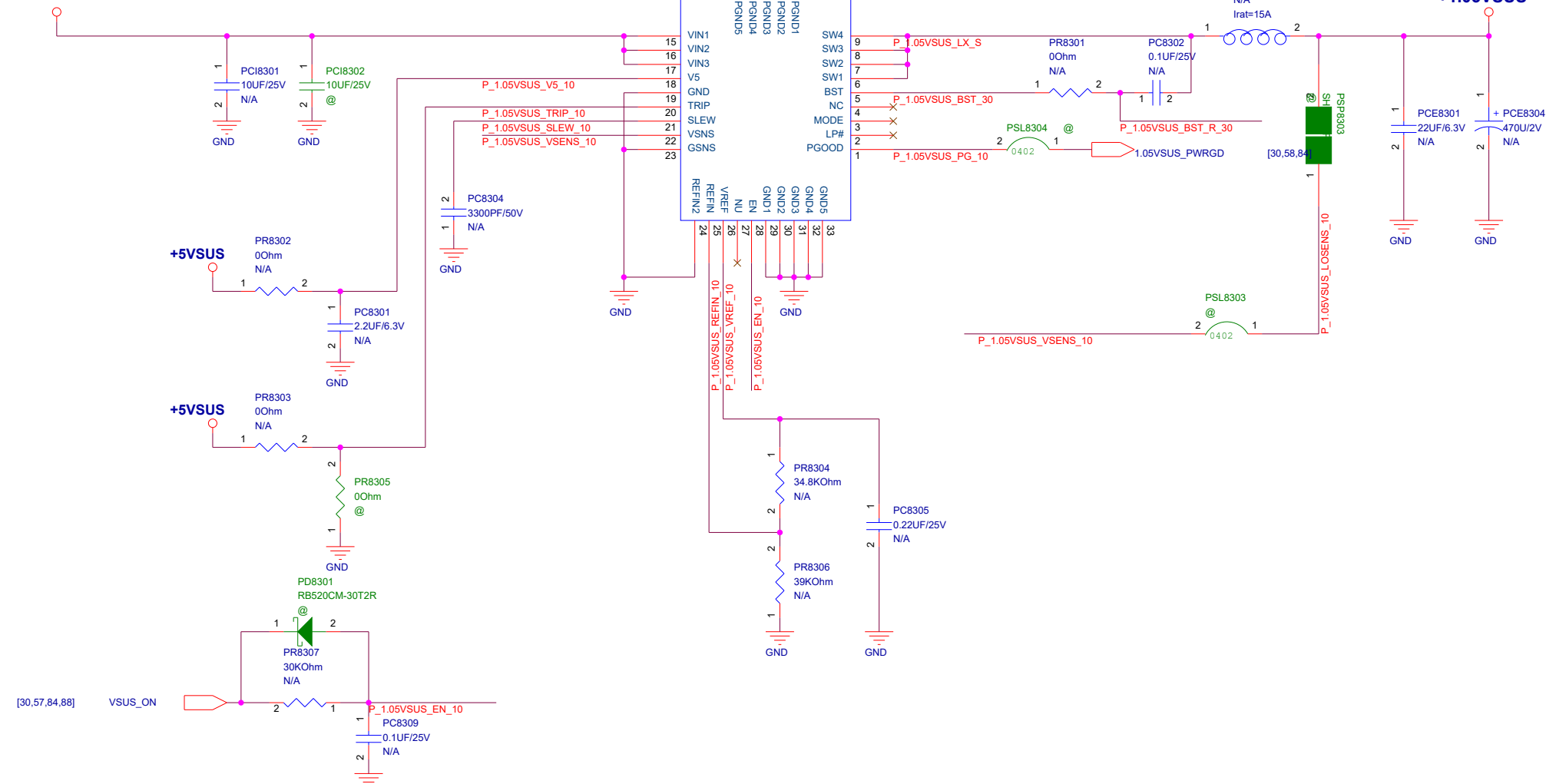
Power	W	W	W
60W	13.5W	13.5W	13.5W
90W	10W	10W	10W
120W	10W	10W	10W
180W	-	28.75W	28.75W
230W	-	24.3W	24.3W



+VCCIO [For CPU]




+1.05VSUS [For PCH]



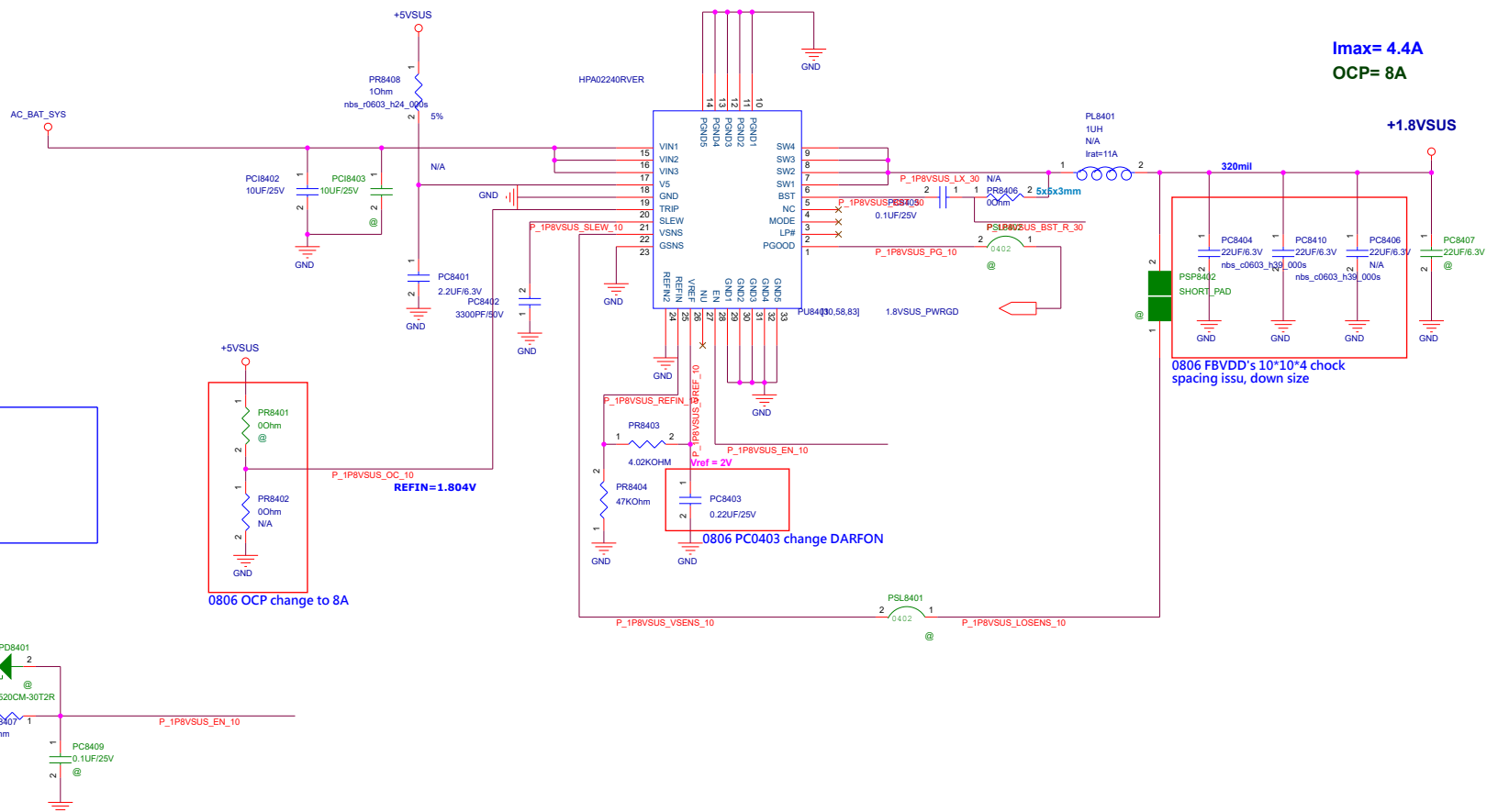
PT840* 請放置 PU8401旁;並請放置Trace 上!




<Variant Name>

		Project Name GX550LXS		Rev R1.0	
Title : PW_+1.OVSUS					
Size A4		Dept.: NB Power team		Engineer: Power RD	
Date: Wednesday, February 19, 2020				Sheet 83 of 103	

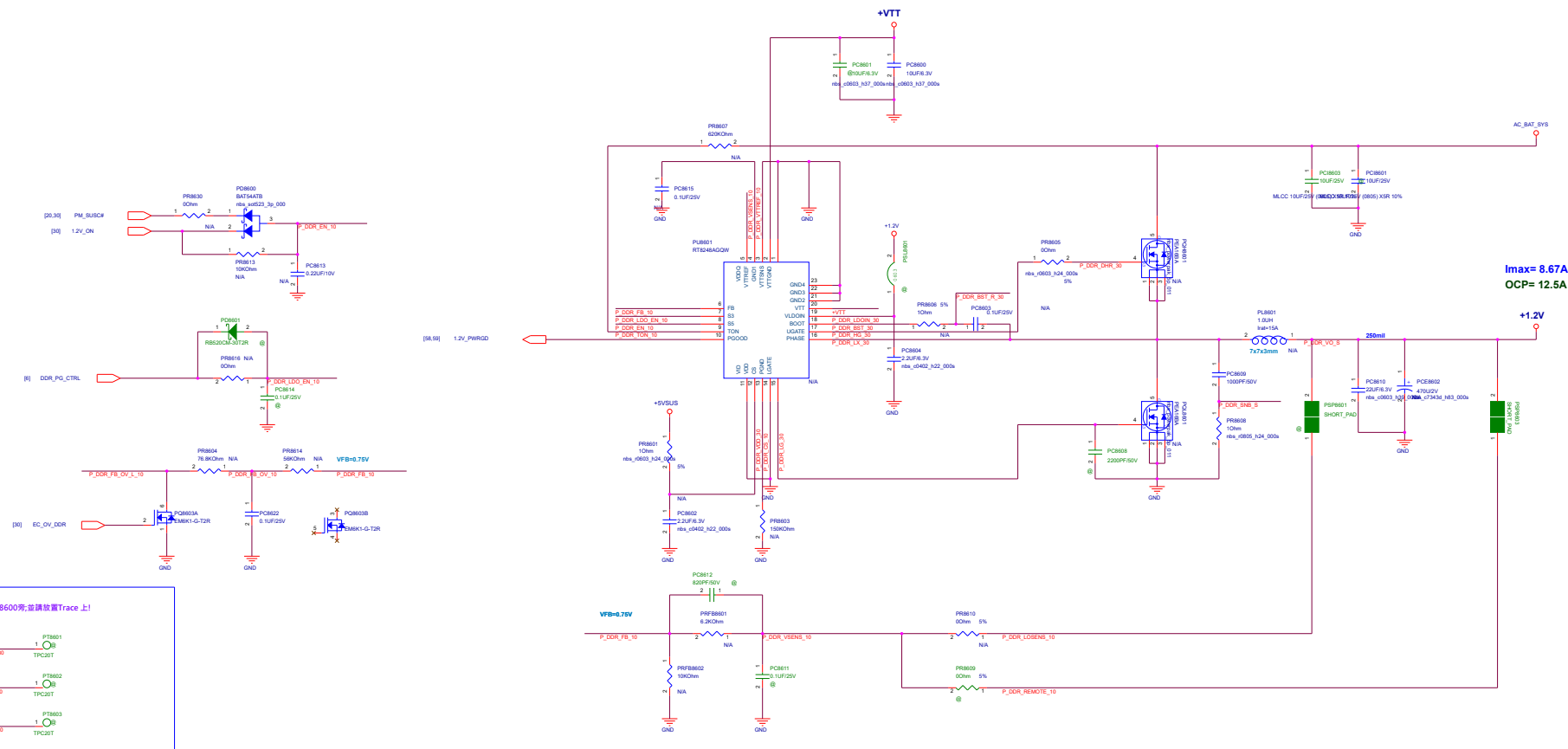
+1.8VSUS [For PCH]



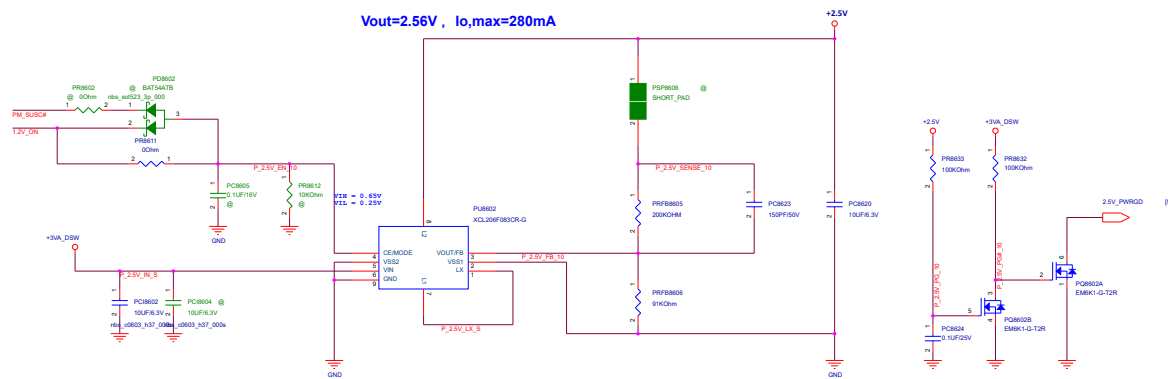
<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size C	Project Name GX701		Rev 1.0
Date: Wednesday, February 19, 2020		Sheet 85 of 103	

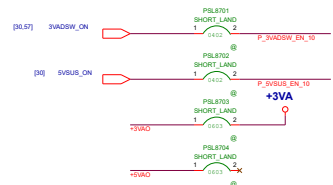
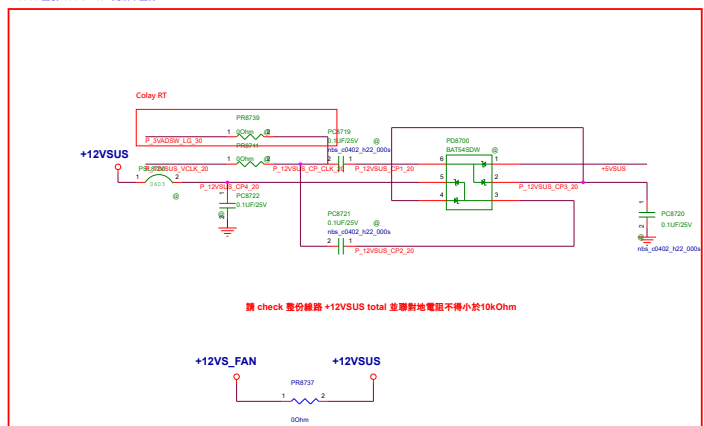
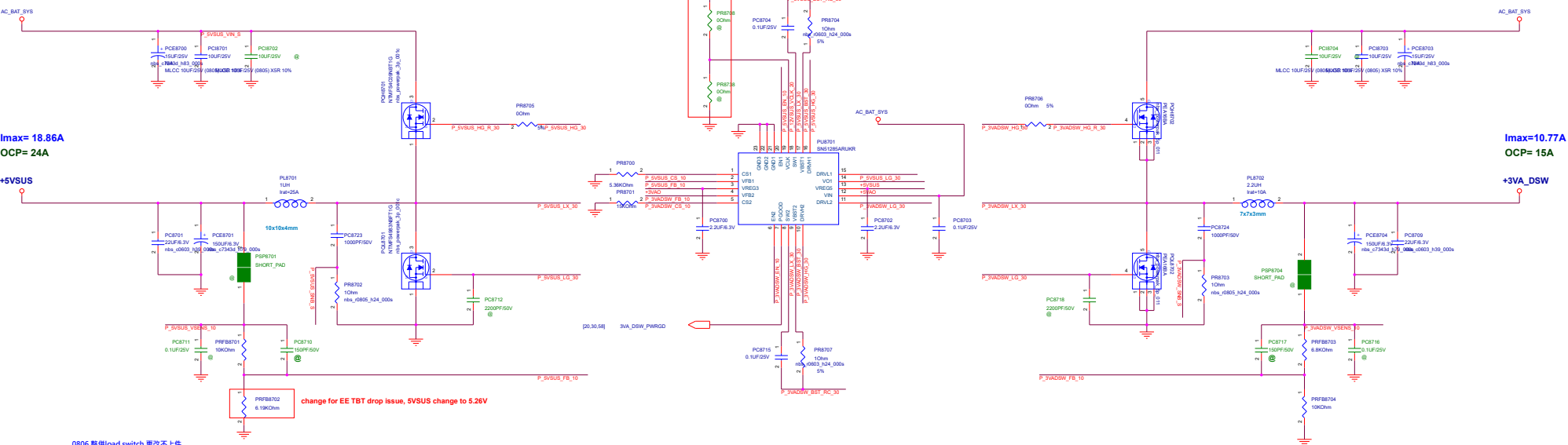
+1.2V / +2.5V [For Memory]



+2.5V BUCK (XCL206)



+3VA_DSW / +5VSUS [System Power]

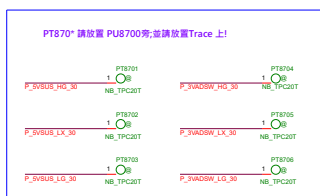


Adaptor Mode (IMVP8)

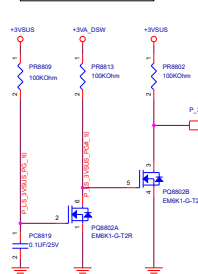
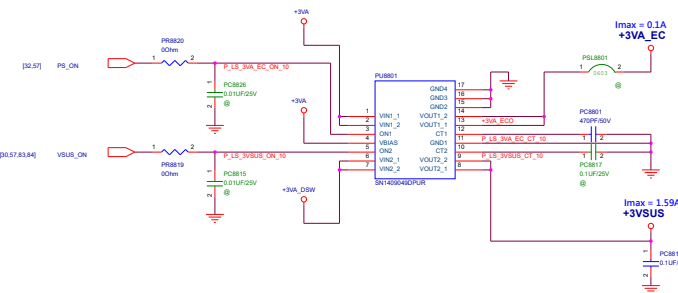
	S0	S3	D33	S4	S6	S5 with USB Charger+
PS_ON	1	-	1	-	1	1
3VADSW_ON	1	-	1	-	1	1
3VSUS_ON	1	-	1	-	1	1
5VSUS_ON	1	-	1	-	1	1
1.35V_ON	1	-	1	-	0	0
SUSC_ECM	1	-	1	-	0	0
SUSB_ECM	1	-	0	-	0	0

Battery Mode (IMVP8)

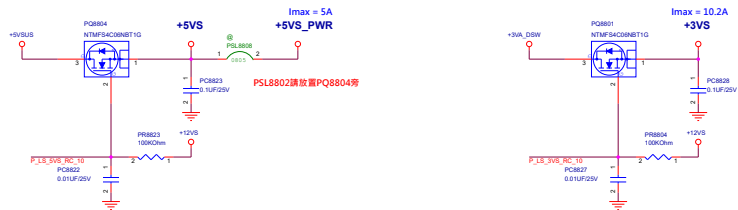
	S0	S3	D33	S4	S6	S5 with USB Charger+
PS_ON	1	-	1	0	0	1
3VADSW_ON	1	-	1	0	0	0
3VSUS_ON	1	-	1	0	0	0
5VSUS_ON	1	-	1	0	0	1
1.35V_ON	1	-	1	0	0	0
SUSC_ECM	1	-	1	0	0	0
SUSB_ECM	1	-	1	0	0	0



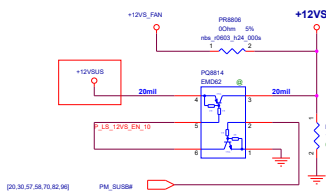
Load Switch



Add for EE

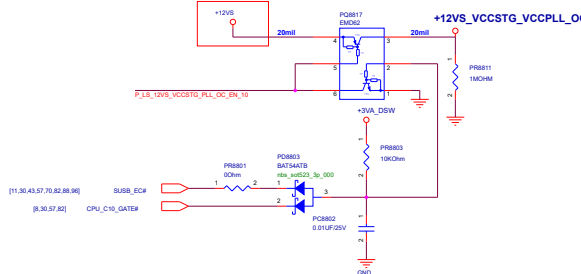
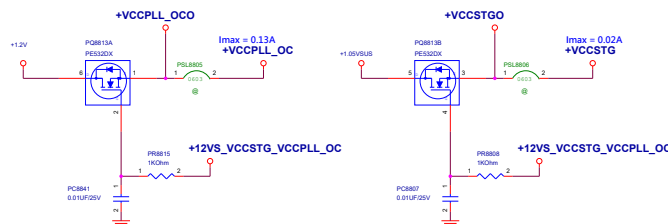
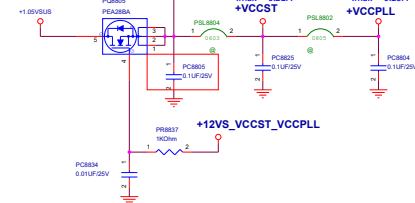
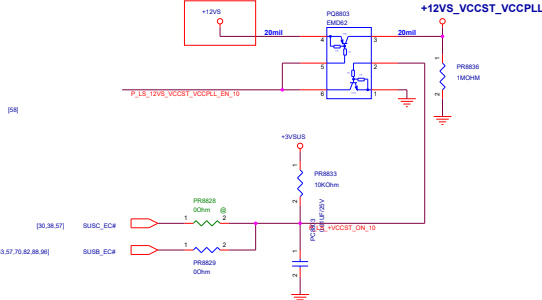
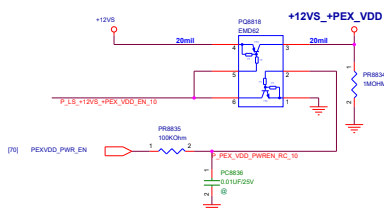
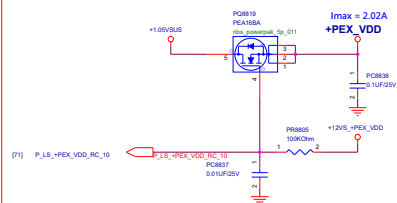


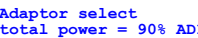
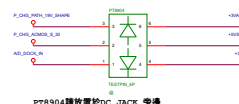
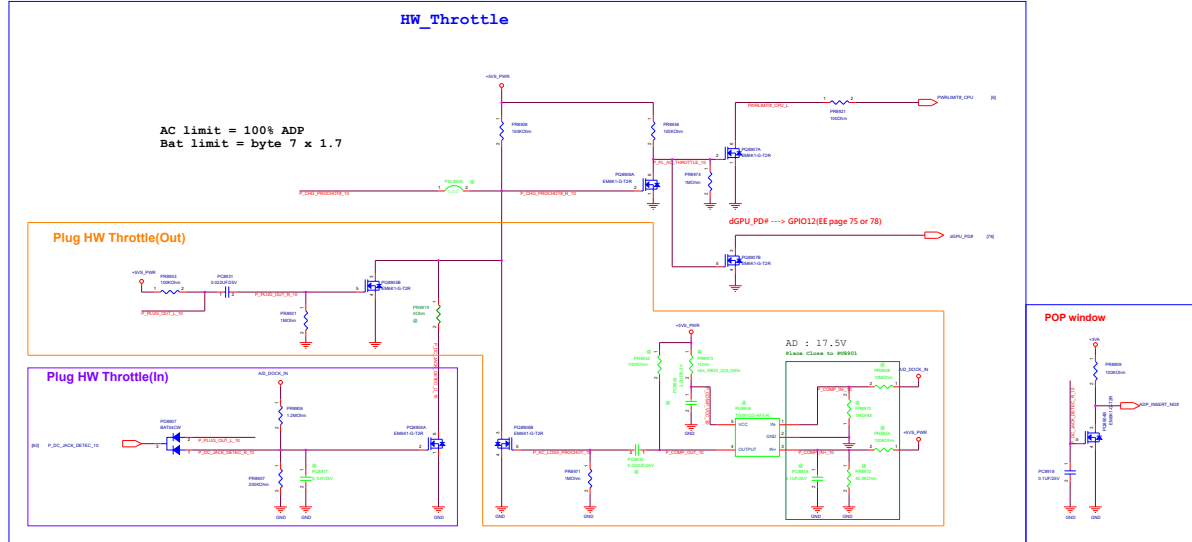
+12VS的Vin 對應BOM表		
	+12VS_FAN	+12VSUS
PR8806	N/A	●
PR8810	●	N/A
PQ8814	●	N/A



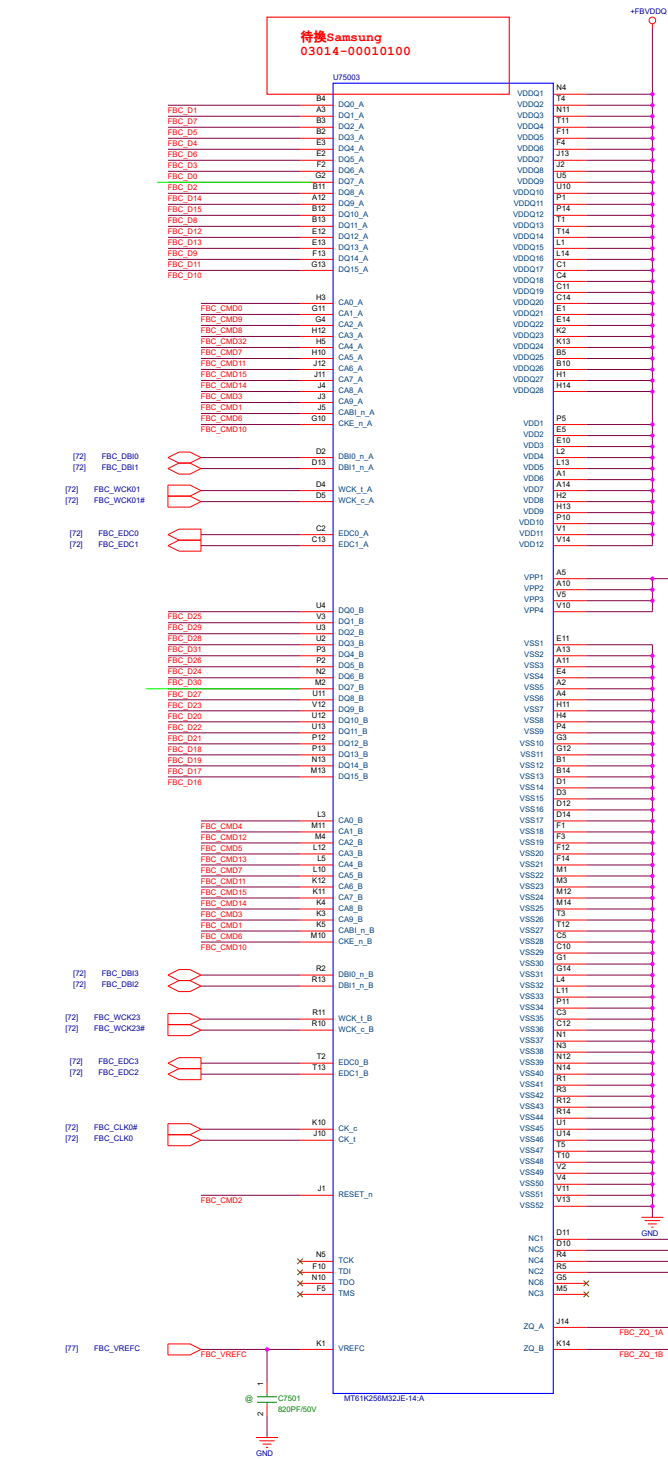
有獨立線路
P97: PW PEX_VDD 時
此處的線路請刪除

PQ8820 - 07G003598010
2nd : 07003-00030800
07003-00030900
棄用 : 07G003000120

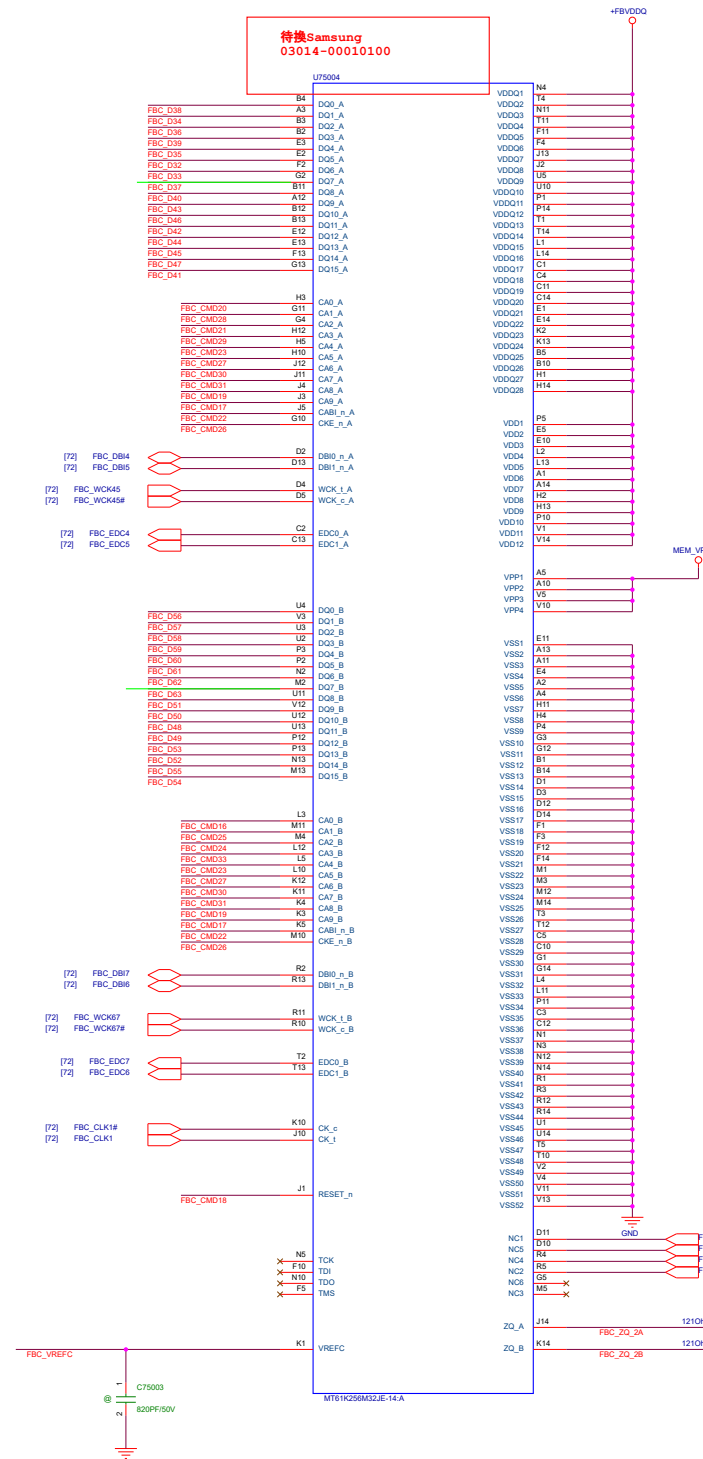


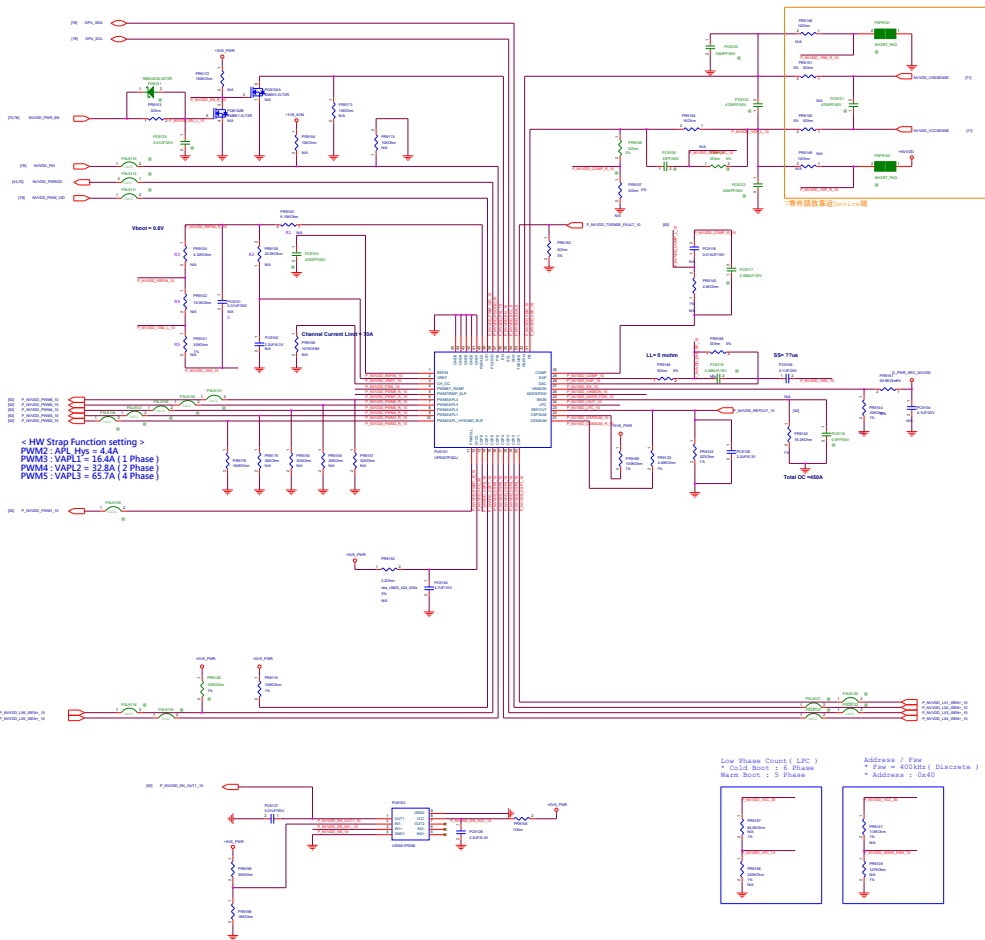
[illegible]

40 Ohm NET
FBC Partition 31..0
MF=1 Mirror

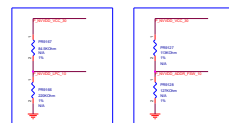


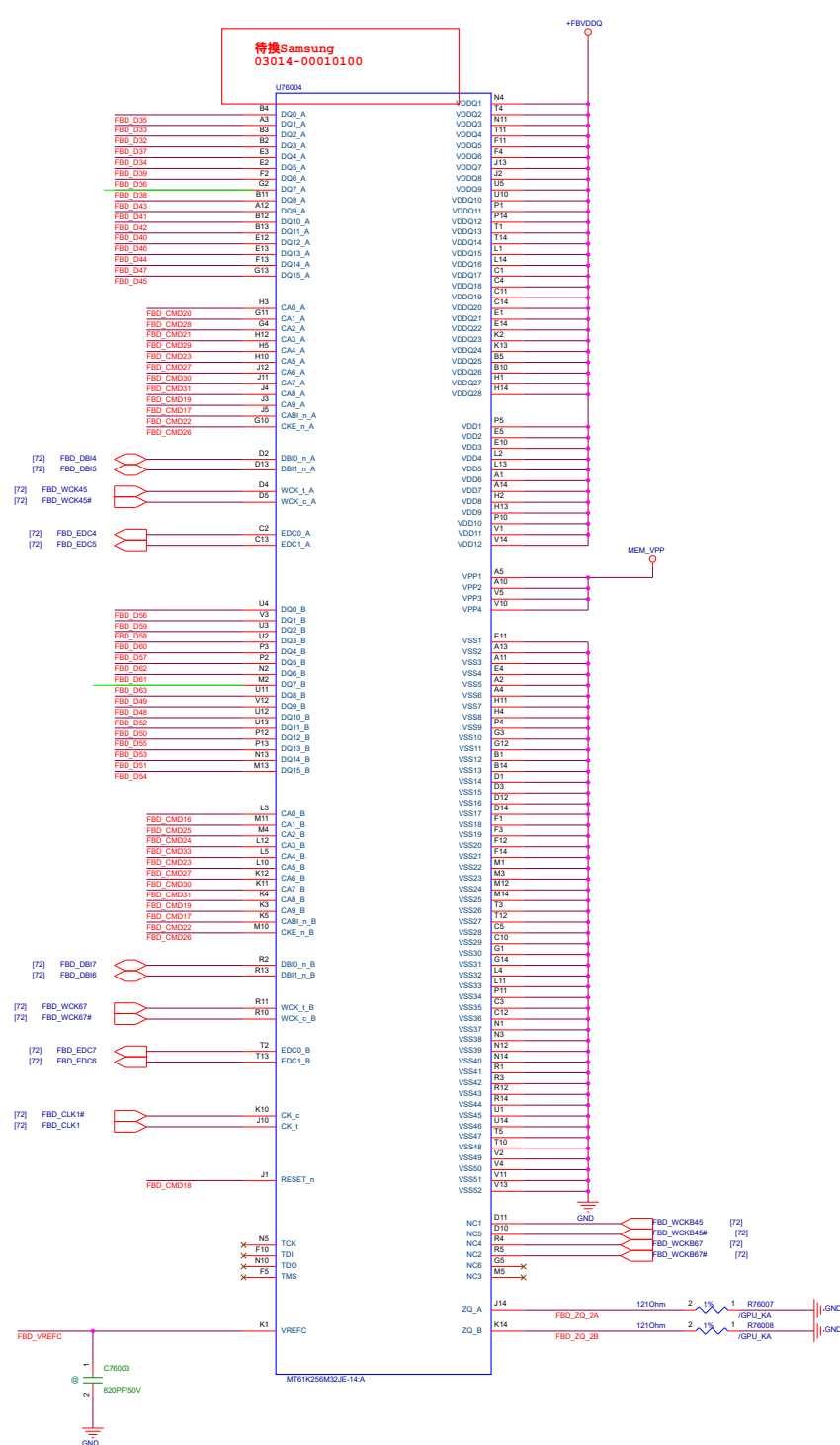
40 Ohm NET
FBC Partition 64..32
MF=0 Normal



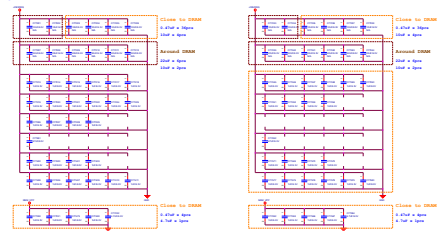


Low Phase Count(LPC)	Address / Fw
* Cold Boot : 6 Phase	* Fw = 400kHz(Discrete)
Warm Boot : 5 Phase	* Address : 0x40

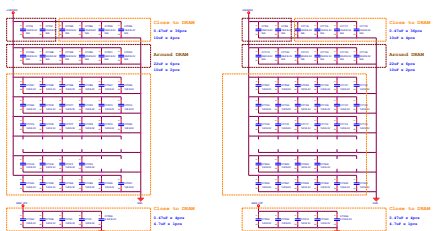




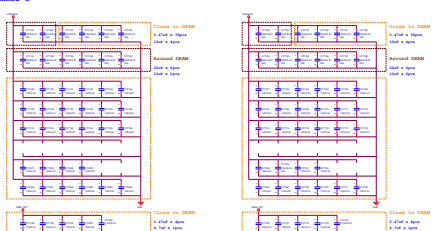
Channel A



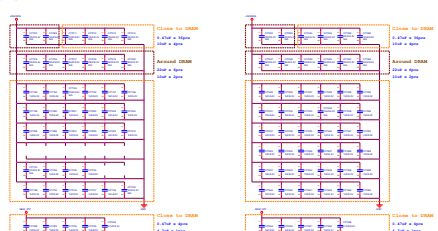
Channel B



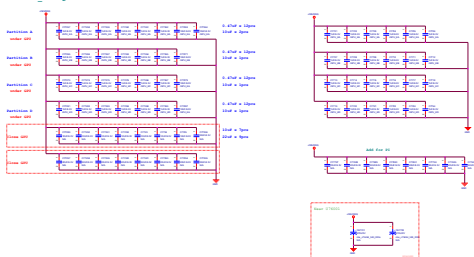
Channel C



Channel D



VRAM FSVDDQ



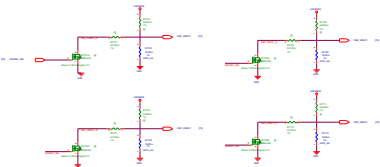
For power sequence measurement

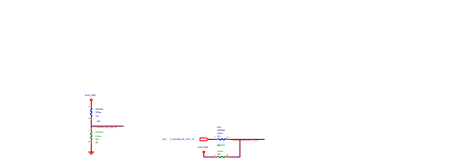
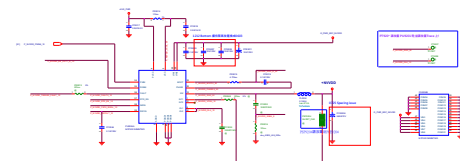
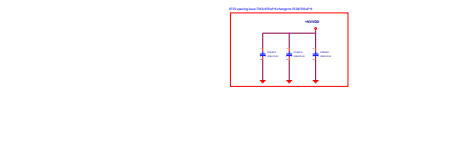
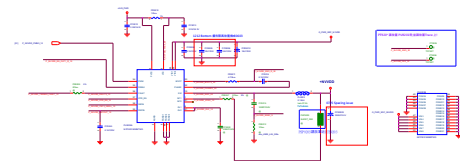
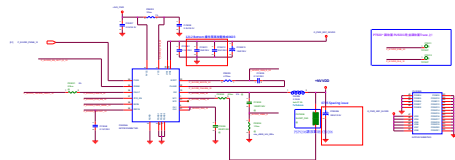
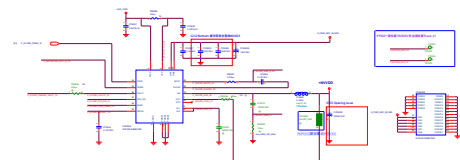
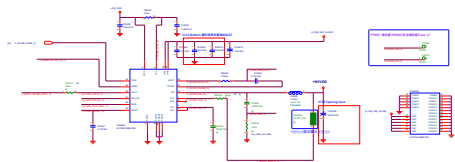
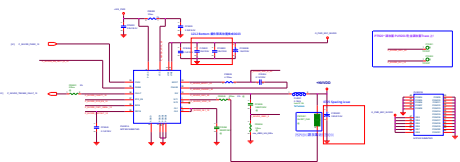


VRAM Thermal Sensor

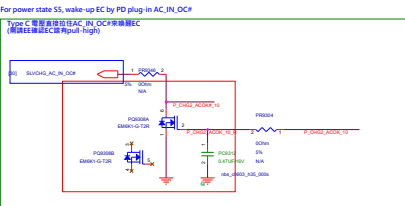
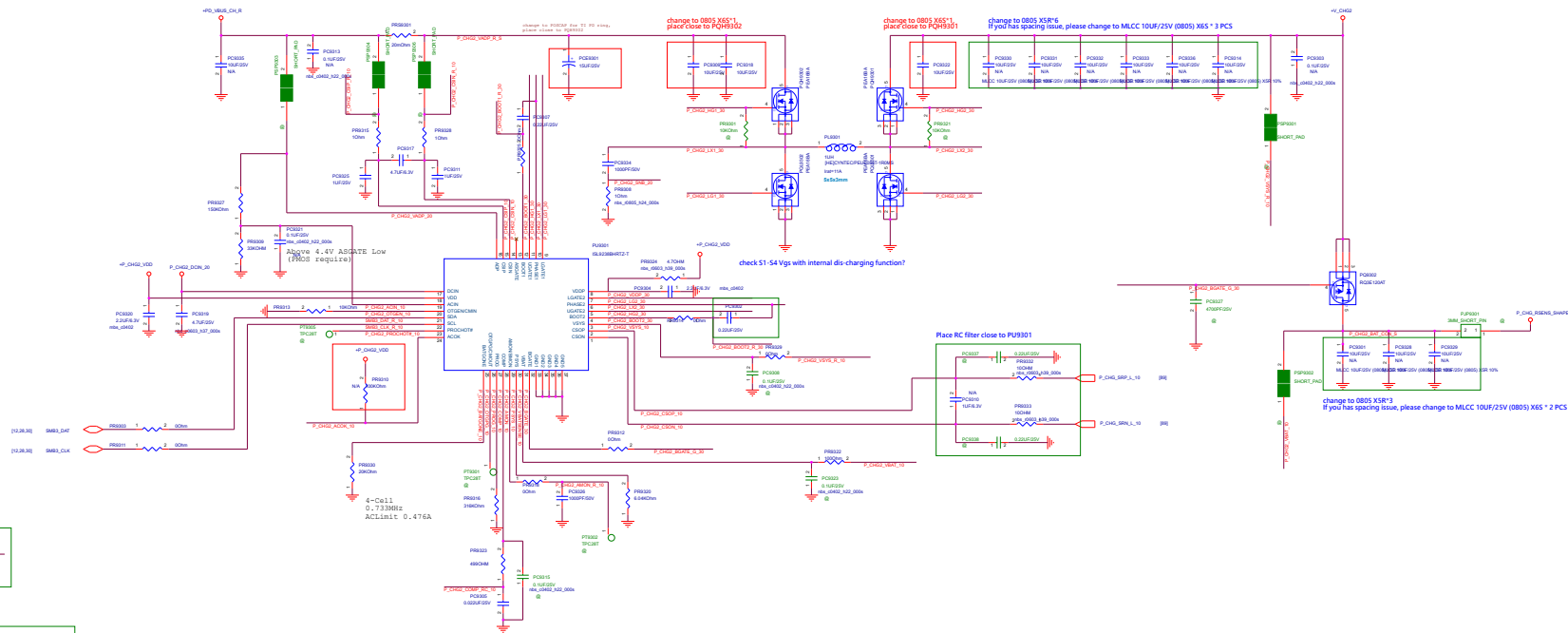
U7701 close to VRAM.

U7703 close to VDDQ.





Charger ISL92388 (NVDC)

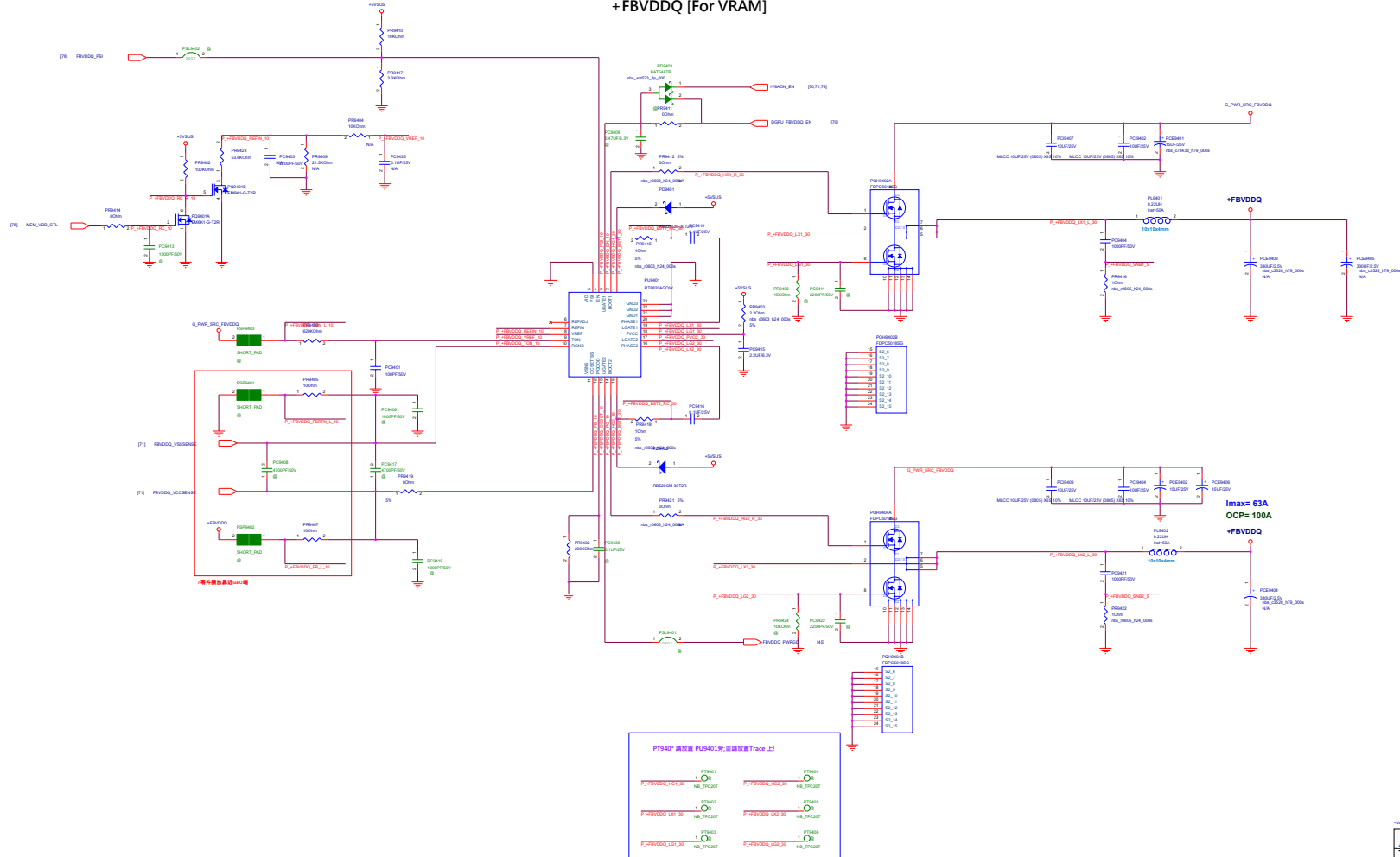


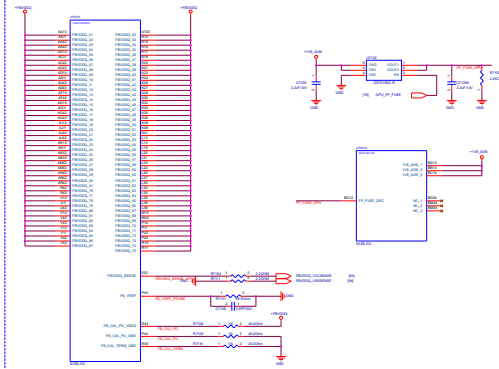
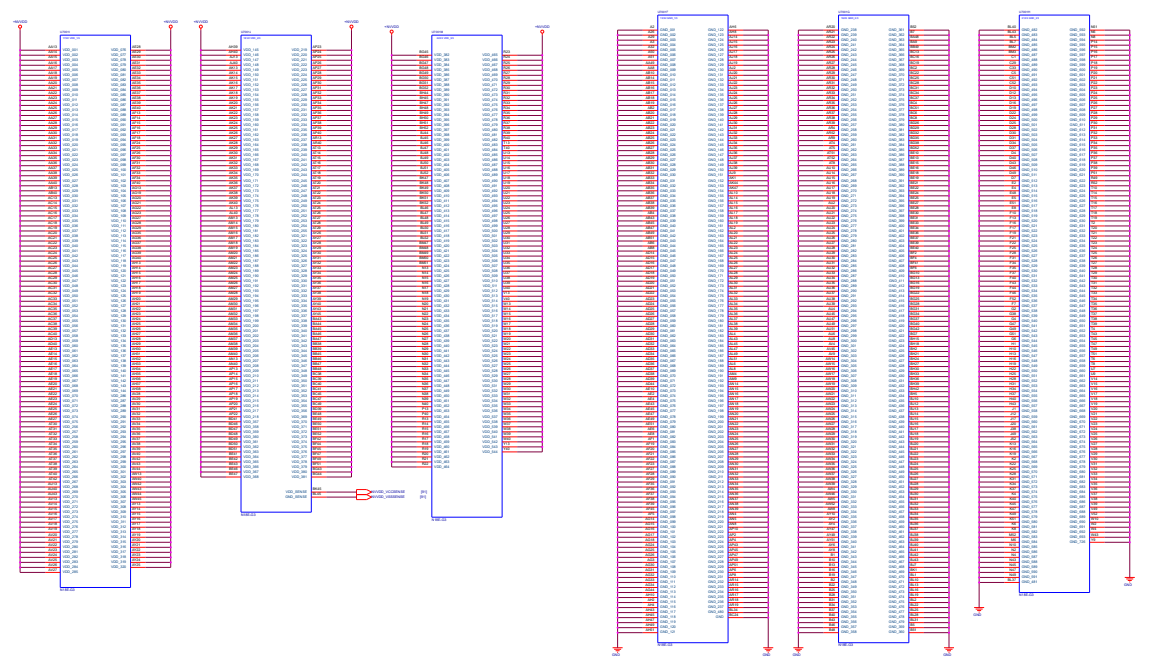
+FBVDDQ [For VRAM]

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.25V
#99404	10KOhm	
#99409	21.5KOhm	
#99423	75KOhm	

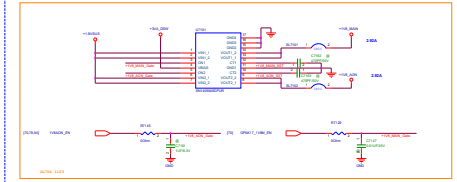
DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.2V
P93404	10XOhm	
P93409	21.5KOhm	
P93423	53.6KOhm	

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.25V	1.2V
F09404	10KOhm	
F09409	16.9KOhm	
F09423	140KOhm	

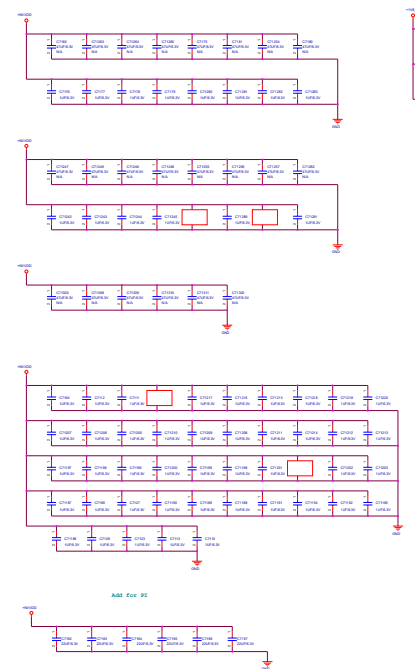
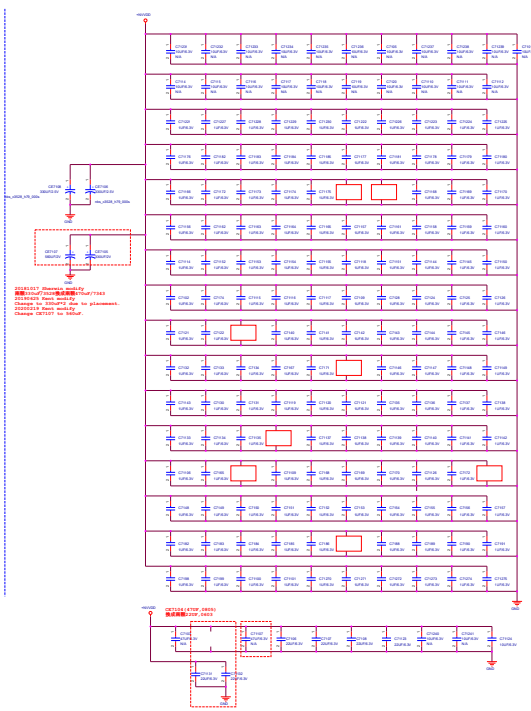
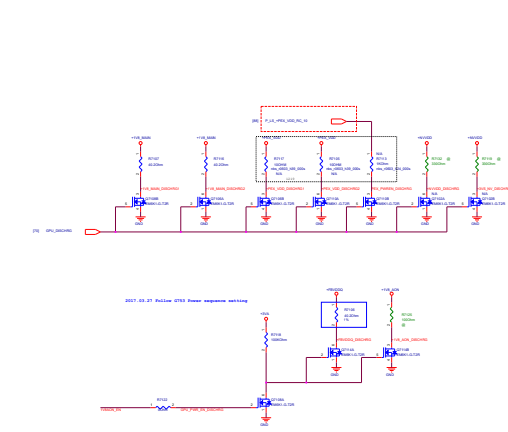





1VB & 3V3 Power Control



Discharge



<Variant Name>

		Project Name		Rev
		GX550LXS		R1.0
Title : PW_PEX_VDD/+1.8V_GPU				
Size Custom	Dept.: NB Power Team		Engineer:	Joe
Date: Wednesday, February 19, 2020			Sheet	95 of 103



Project Name

GX550LXS

Rev

R1.0

Title : **Type C LDO 3V3**

Size

Custom

Dept.: **ASUSTeK COMPUTER INC.** **Engineer:** **Joe**

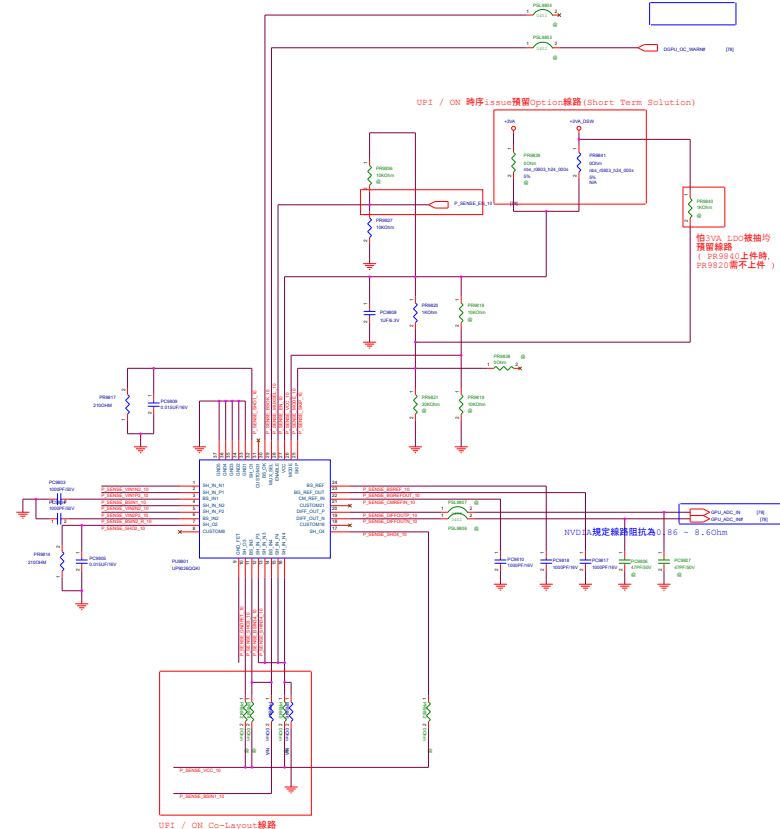
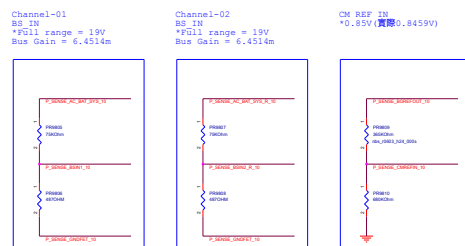
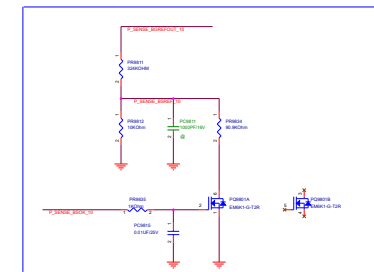
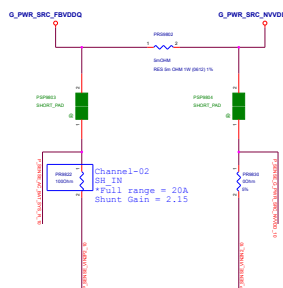
Date: **Wednesday, February 19, 2020**

Sheet

97

of

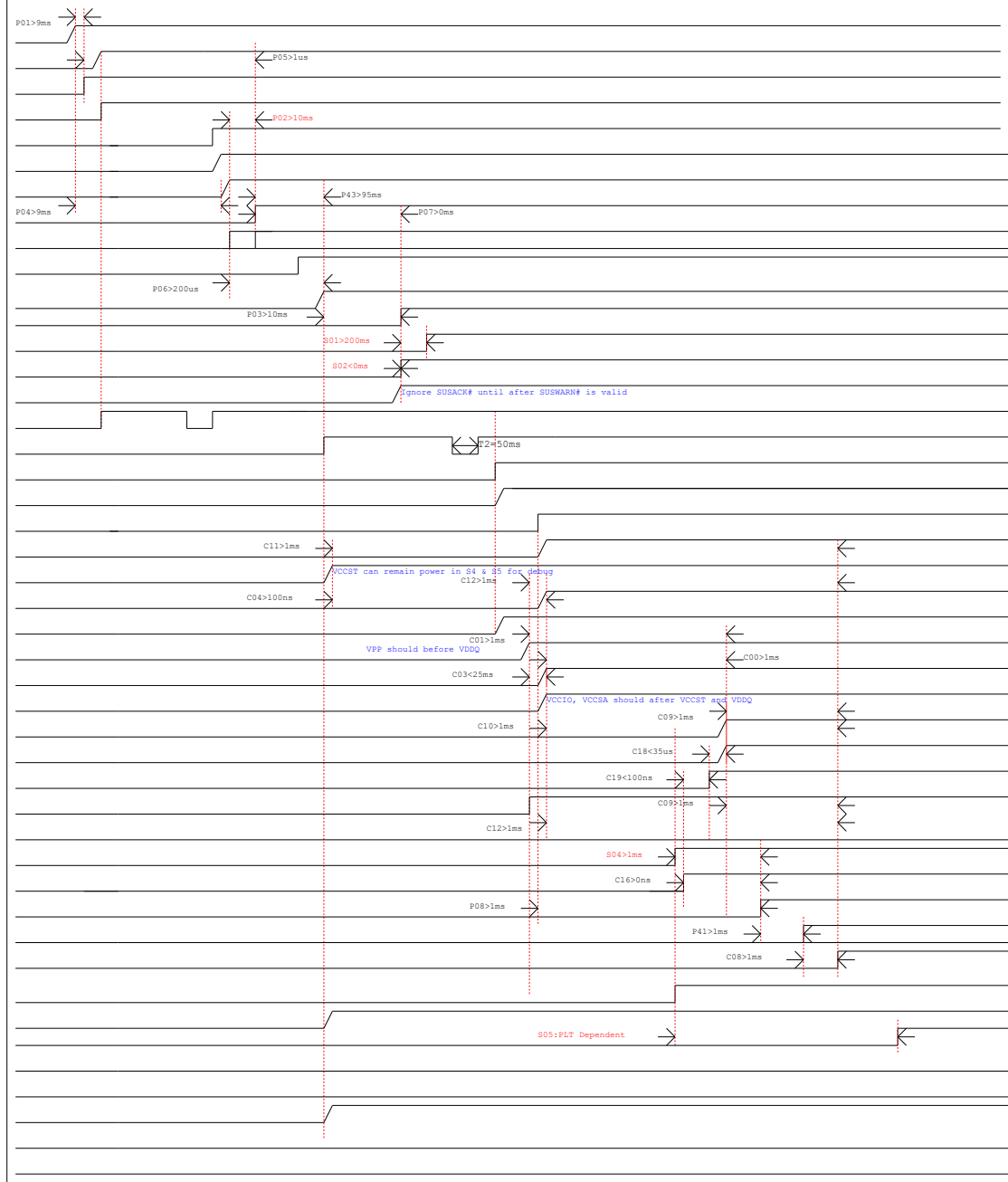
103



—

DC-IN Mode

C:CPU (+RTCBAT)+3VA_RTC
P:PCH (AC_BAT_SYS)+3VA/+5VA
S:PLT (+3VA_RTC) RTCRST# (PCH)
Power (Power) AC_IN_OC# (EC)
Signal (EC) PS_ON (+3VA_EC)
(PS_ON)+3VA_EC (EC)
(3VADSW_ON)+3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON)+1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR_Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#)+12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#)+12VS/+5VS/+3VS
(VSUS_ON)+1.0V_VCCST, VCCPLL (VCCST_PWRGD)
(+VCCIO)+VCCSTG
(1.2V_ON)+2.5V (2.5V_PWRGD)
(1.2V_ON)+VDDQ_CPU (1.2V_PWRGD)
(+12VS)+VCCPLL_OC
(SUSB_EC#)+VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD)+VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL)+0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPU_PWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON)+VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT

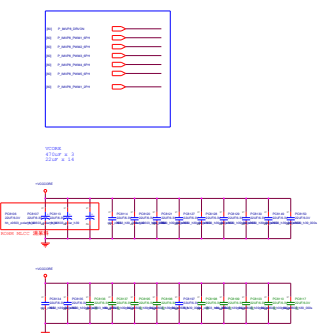
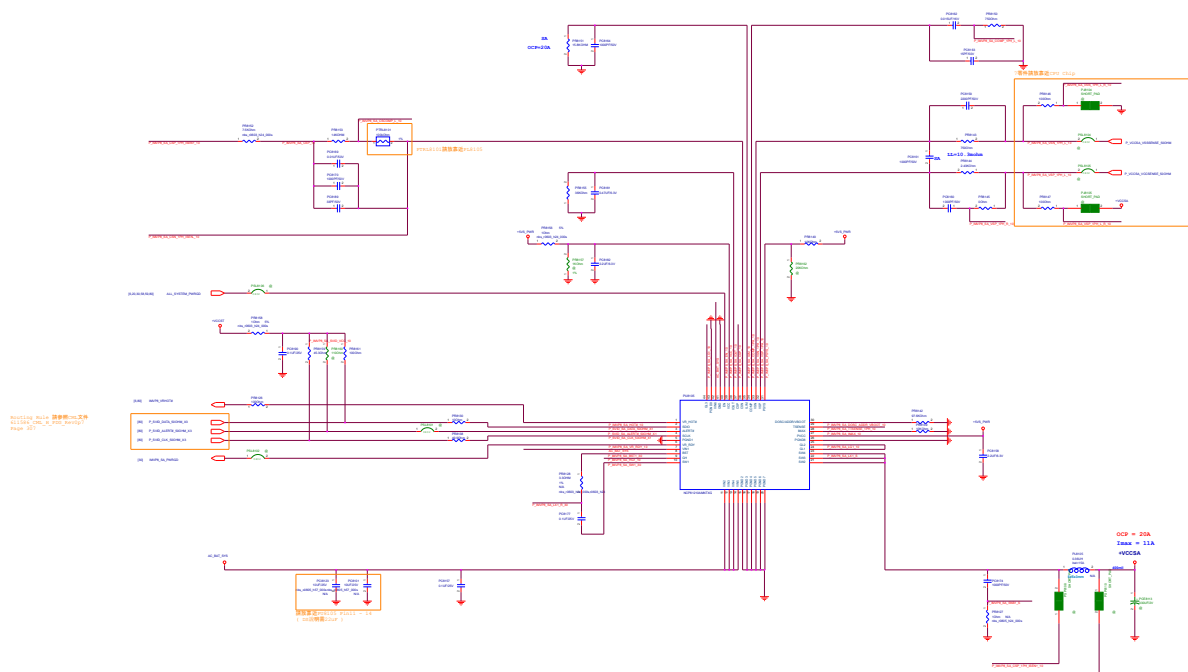
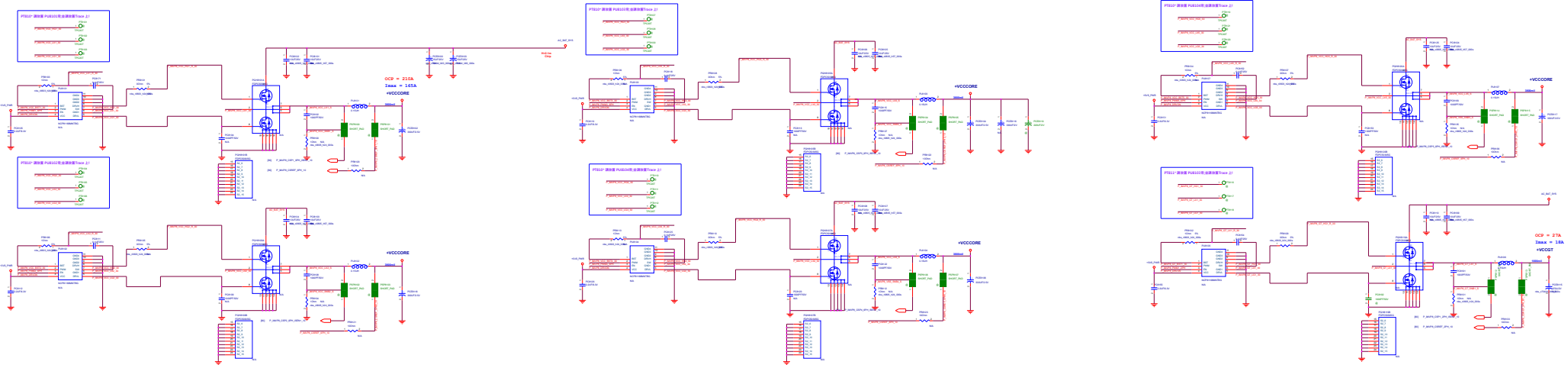


CFL H Power Sequence
(DC mode)

GX502GX R1.1 SKU Table

Option	PCB	SKU	CPU	Power	DIMM	VRAM			

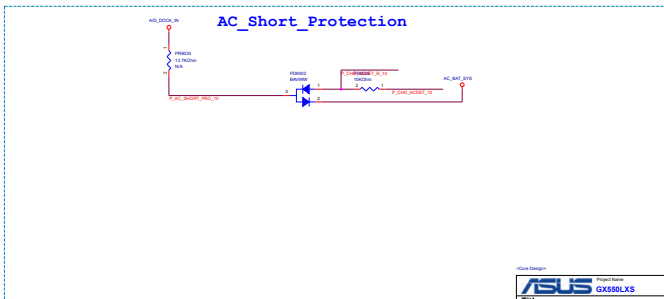
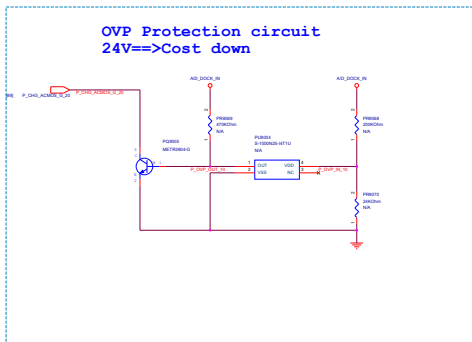
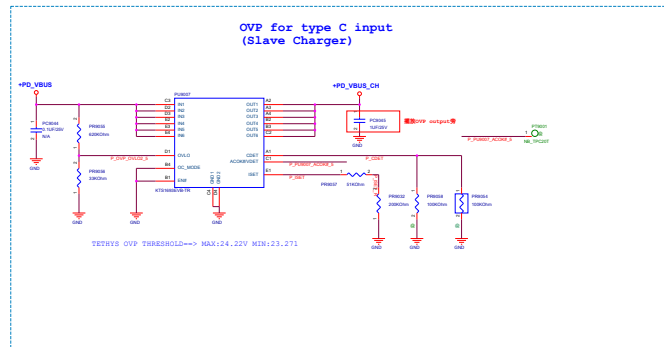
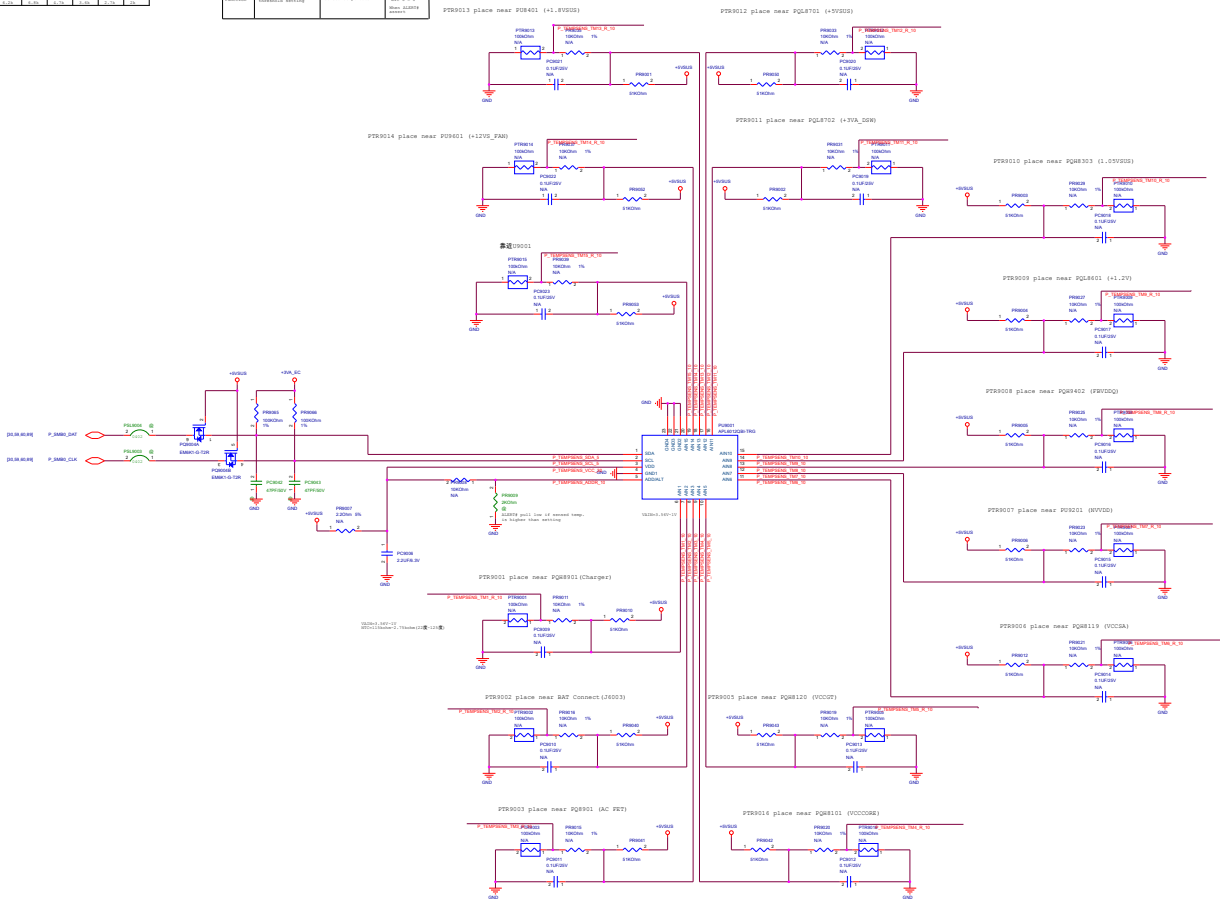
		Title : GX502GX SKU Table R1.1	
Product Name COMPUTER		Engineer: EE	
Part No. : GX550LXS			
Rev. : 01.0			



Address Selection Table									
Address	Bank	Bank	Bank	Bank	Bank	Bank	Bank	Bank	Bank
0x0000	0	0	0	0	0	0	0	0	0
0x0001	0	0	0	0	0	0	0	0	0
0x0002	0	0	0	0	0	0	0	0	0
0x0003	0	0	0	0	0	0	0	0	0
0x0004	0	0	0	0	0	0	0	0	0
0x0005	0	0	0	0	0	0	0	0	0
0x0006	0	0	0	0	0	0	0	0	0
0x0007	0	0	0	0	0	0	0	0	0
0x0008	0	0	0	0	0	0	0	0	0
0x0009	0	0	0	0	0	0	0	0	0
0x000A	0	0	0	0	0	0	0	0	0
0x000B	0	0	0	0	0	0	0	0	0
0x000C	0	0	0	0	0	0	0	0	0
0x000D	0	0	0	0	0	0	0	0	0
0x000E	0	0	0	0	0	0	0	0	0
0x000F	0	0	0	0	0	0	0	0	0

Register Address									
Address	Bank	Bank	Bank	Bank	Bank	Bank	Bank	Bank	Bank
0x0000	0	0	0	0	0	0	0	0	0
0x0001	0	0	0	0	0	0	0	0	0
0x0002	0	0	0	0	0	0	0	0	0
0x0003	0	0	0	0	0	0	0	0	0
0x0004	0	0	0	0	0	0	0	0	0
0x0005	0	0	0	0	0	0	0	0	0
0x0006	0	0	0	0	0	0	0	0	0
0x0007	0	0	0	0	0	0	0	0	0
0x0008	0	0	0	0	0	0	0	0	0
0x0009	0	0	0	0	0	0	0	0	0
0x000A	0	0	0	0	0	0	0	0	0
0x000B	0	0	0	0	0	0	0	0	0
0x000C	0	0	0	0	0	0	0	0	0
0x000D	0	0	0	0	0	0	0	0	0
0x000E	0	0	0	0	0	0	0	0	0
0x000F	0	0	0	0	0	0	0	0	0

PROTECTION




```

C:CPU
P:PCCH
S:PLT
Power
Signal

(+RTCBAT)+3VA/+5VA
(AC_BAT_SYS)+3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PN_ON)+3VA_EC (EC)
(3VADSW_ON)+3VA_DSW (3VA_DSW_FWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON)+1.0VSUS_VCCPRIM (1.0VSUS_FWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWRN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR_Switch) PWR_SW# (EC)
(EC) PM_FWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#)+12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#)+12VS/+5VS/+3VS
(SUSB_EC#)+1.0V_VCCST,VCCPLL
(SUSB_EC#)+VCCIO, (+12VS)+VCCSTG
(1.2V_ON)+2.5V (2.5V_FWRGD)
(1.2V_ON)+VDDQ_CPU (1.2V_FWRGD)
(+12VS)+VCCPLL_OC
(SUSB_EC#)+VCCIO (VCCIO_FWRGD)
(ALL_SYSTEM_FWRGD)+VCCSA (IMVP8_FWRGD)
(DDR_VTT_CTRL)+0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_FWRGD (AND)
(Power) IMVP8_FWRGD
(AND) ALL_SYSTEM_FWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_FWRGD) VCCST_FWRGD_CPU (CPU)
(EC) PM_FWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUFWRGD (CPU)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON)+VCCCORE (IMVP8_FWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCIO

```

CFL H Power Sequence (AC mode)

The diagram illustrates the power sequence for CFL H in AC mode. Key timing constraints include:

- P01**: >9ms
- P05**: >1us
- P02**: >10ms
- P04**: >9ms
- P43**: >95ms
- P07**: >0ms
- P06**: >200us
- P03**: >10ms
- S01**: >200ms
- S02**: <0ms
- Ignore SUSACK# until after SUSWARN# is valid**
- P2**: =50ms
- C11**: >1ms
- VCCST can remain power in S4 & S5 for debug**
- C12**: >1ms
- C04**: >100ns
- VPP should be before VDDQ**
- C01**: >1ms
- C03**: <25ms
- VCCI0, VCCSA should after VCCST and VDDQ**
- C10**: >1ms
- C09**: >1ms
- C18**: <35us
- C19**: <100ns
- C09**: >1ms
- C12**: >1ms
- S04**: >1ms
- C16**: >0ms
- P08**: >1ms
- P41**: >1ms
- C08**: >1ms
- S05: FLT Dependent**